12 19 MIXER 25 37 42 KEYBOARD 53 57

DECEMBER 85 - FEBRUARY 86 PRICE 75p

Electronics

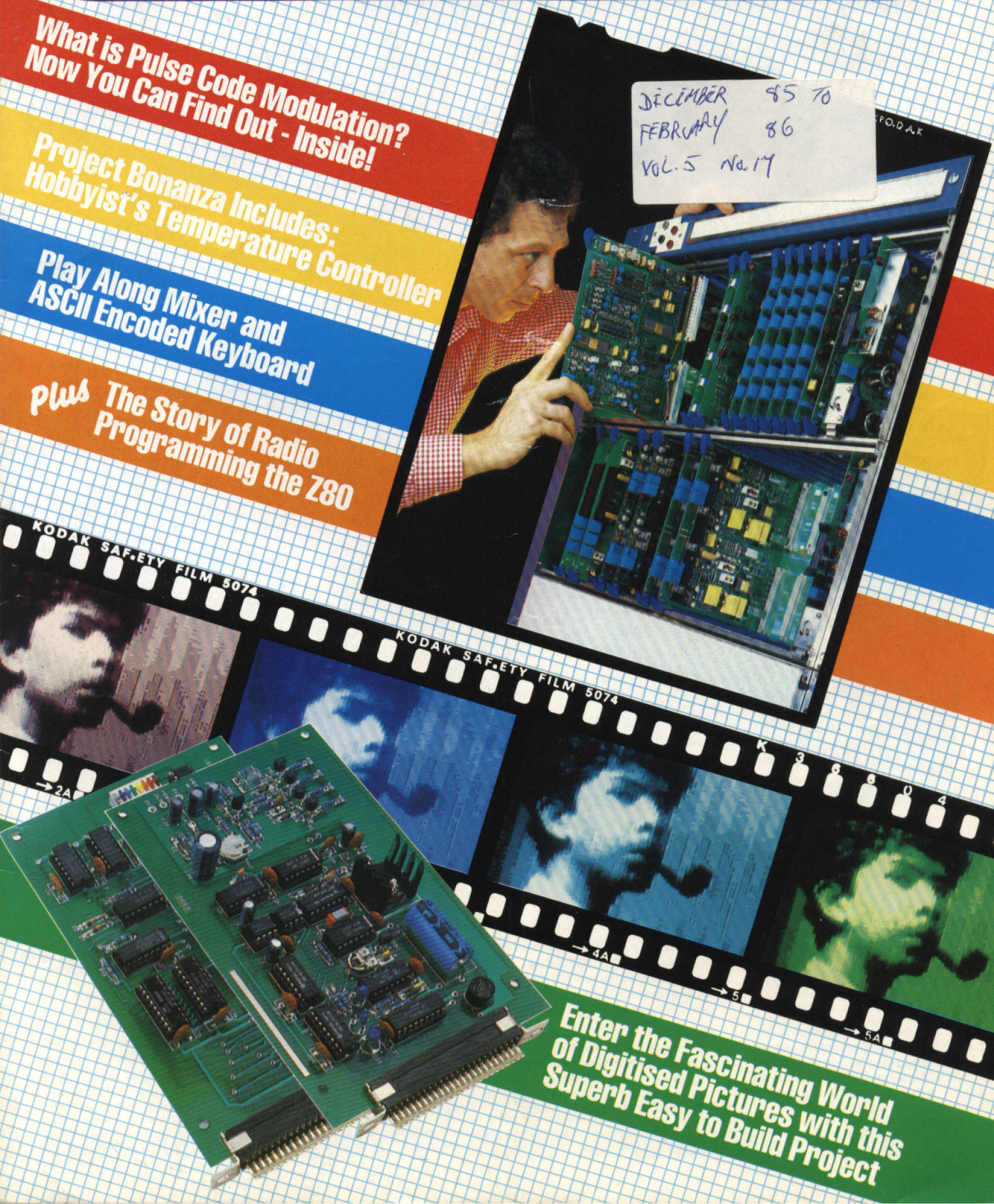
THE MAPLIN MAGAZINE

What is Pulse Code Modulation? Now You Can Find Out - Inside!

Project Bonanza Includes: Hobbyist's Temperature Controller

Play Along Mixer and ASCII Encoded Keyboard

plus The Story of Radio Programming the Z80



Enter the Fascinating World of Digitised Pictures with this Superb Easy to Build Project

DECEMBER 85 TO FEBRUARY 86 VOL. 5 No. 17

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Volume 5 Number 17

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Electronics
THE MAPLIN MAGAZINE

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Save television picture stills on tape or disk in digital format! If used with a monochrome TV camera, your computer could have the power of sight – opening up all sorts of possibilities in the area of image recognition and comparison, sophisticated security monitoring – your own imagination is the limit. The Digitiser requires the host computer to run in machine code to preserve a reasonably quick picture scanning time, but a controller is also described that enables programs to be written in BASIC.

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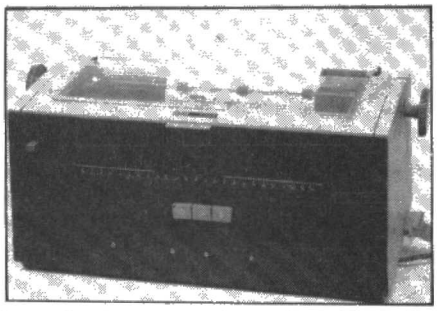

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Hobbyist's Temperature Controller 37

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At last, a complete computer terminal keyboard unit at an affordable price. The project comprises all the electronics for the generation of all the standard ASCII encoded characters, outputted in parallel form.

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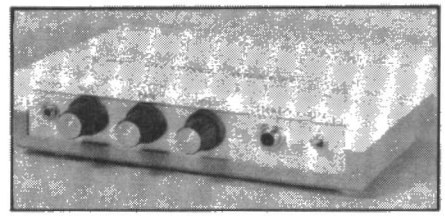

A simple, easy to build project which mixes the output from your electric guitar or organ, etc., together with a pre-recorded music source for your stereo system. Now you can play along to your favourite records or tapes.

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We very much regret that part 10 of the series First Base, and part 5 of Project Fault Finding, have had to be omitted from this issue due to lack of space.

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Editor	Roy Smith
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Technical Editors	Robert Kirsch, Dave Goodman
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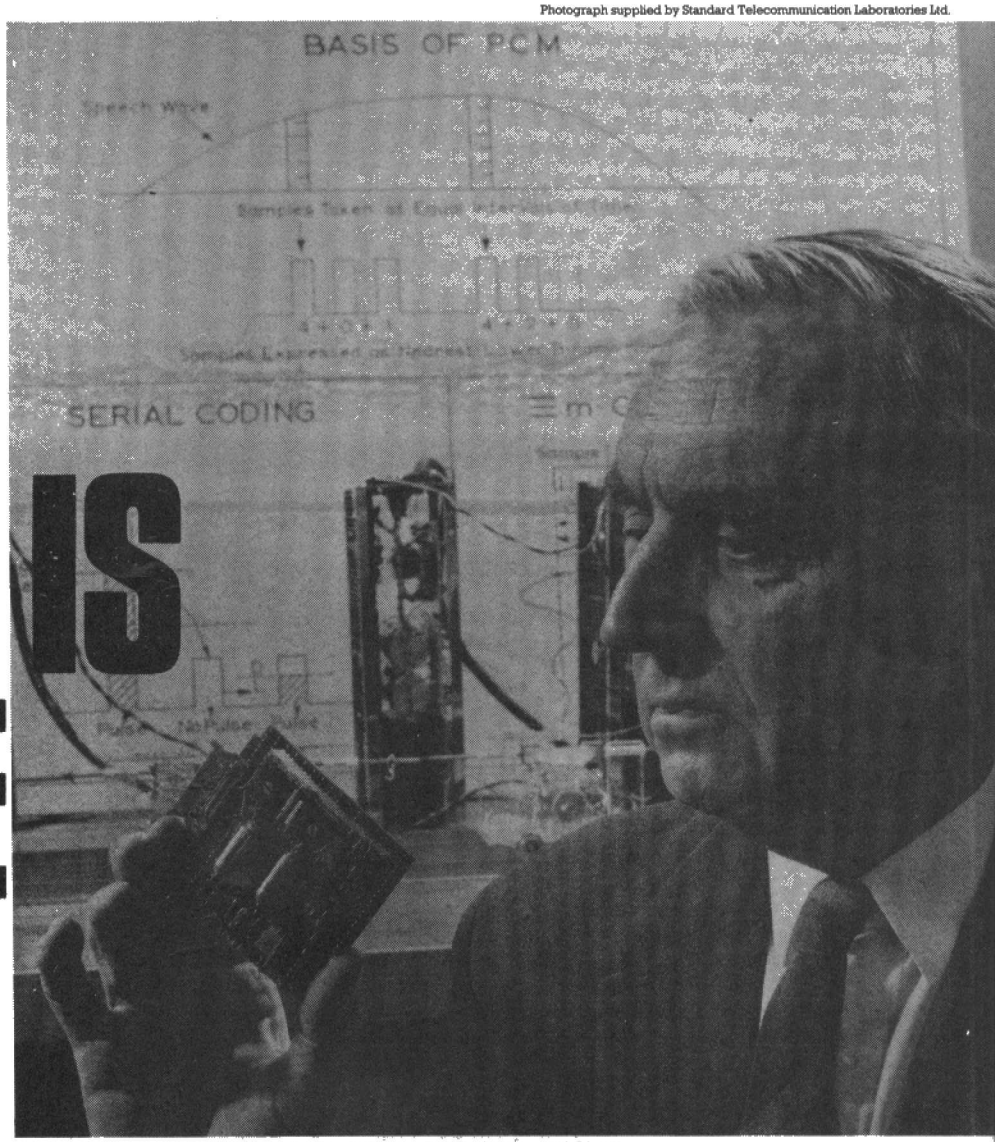


Dr. Alec Harley Reeve

WHAT IS PULSE CODE MODULATION?

by D. Stewart

Digital Transmission of Speech is a complex subject. Read on to find out more . . .

There is nothing new about Pulse Code Modulation (PCM). The technique was known in the 1930's but the technology did not exist to implement the principles. Some give the credit to an Englishman, one Alec Reeves who was working for the Standard Telephones & Cables (STC) company in their Harlow laboratories during 1938 – others to a Frenchman, but whichever side you take there is no doubt that this technique is most important in digital transmission which is replacing analogue transmission rapidly.

Most people are familiar with Amplitude Modulation (AM) and Frequency Modulation (FM). As a quick revision, Figure 1 shows how an audio signal amplitude modulates a radio frequency carrier. Similarly, Figure 2 shows a frequency modulated carrier. If we choose to use pulse techniques, there is a choice of Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), Pulse Width Modulation (PWM) and Pulse Code Modulation (PCM). Figure 3 shows how an audio signal amplitude modulates a train of pulses to give a PAM signal. Figure 4 shows how an audio signal can be described using pulses of different widths (PWM). Or we can alter the position of the pulses as in Figure 5 to give a PPM encoded signal. By far the most popular is PCM which is easier to implement than some of the others and also offers greater flexibility.

The main advantage of digital transmission, whether by radio or cable, is its immunity to noise. If an amplitude modulated signal suffers from noise interference, then the demodulated audio signal is distorted, as shown in Figure 6. Although the PAM signal in Figure 3 is a digital system in that it employs pulses, it is amplitude modulated and hence suffers the noise problems of any amplitude modulated wave. However, in a pulse system where the pulse heights are constant and some other method is used to code the signal, noise immunity will be greater, provided the noise does not exceed the threshold of the detector.

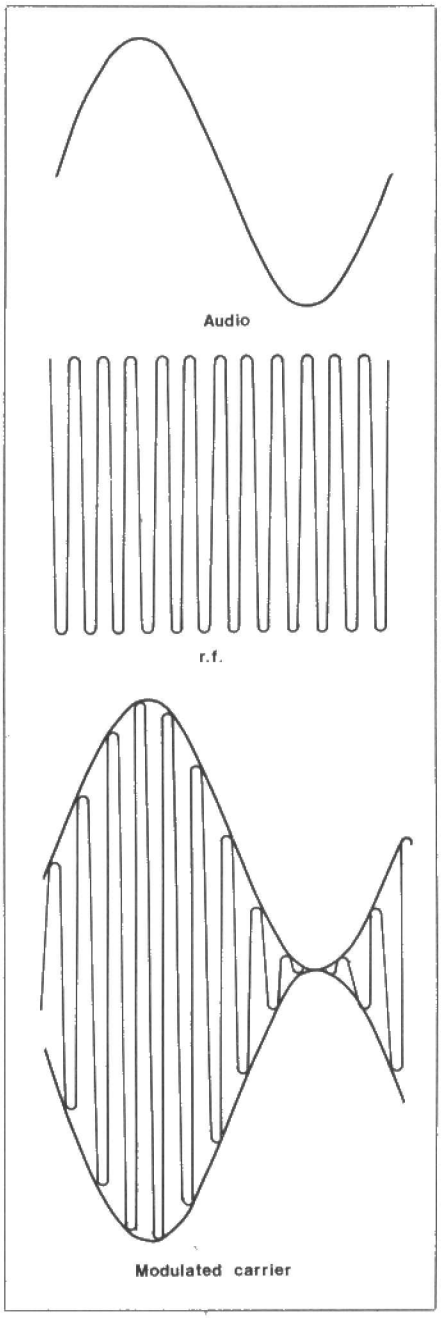


Figure 1. Amplitude Modulation

Figure 7 shows a pulse train which has got a bit ragged during transmission. Provided the regenerator can detect the presence of a pulse, it will replace the ragged one with a new, clean pulse.

Data transmission is by digital pulses; therefore the advantage of converting analogue signals like speech and television into a digital signal is that these analogue signals can then use the same transmission network. The main disadvantage of converting analogue signals into digital signals is that digital systems are hungry for bandwidth. For instance, a typical 4kHz speech channel when encoded in digital form requires around 28kHz depending on the method of coding. Various methods exist for reducing the bandwidth by making the coding more complex, hence increasing the cost of the encoder.

Principles of PCM

With reference to Figure 8, if a waveform is sampled as for PAM and a binary value assigned to each quantity or sample, then only the binary code need be transmitted. The processing of samples and assigning values is called pulse code modulation. The sampling process is called quantisation. In Figure 8, eight positive levels and eight negative levels have been selected. This is called 'Folded Binary' and the first digit of every code indicates the sign (direction) of the waveform; 1 for positive going, 0 for negative going. The remaining three bits are mirror images and give the required eight levels ($2^3 = 8$). If along the x axis (the time axis) we took samples at every possible moment, we could reconstruct the waveform faithfully. But this would mean transmitting an enormous number of bits, hence increasing the bandwidth of the transmission system. We have to manage with fewer samples, which leads to quantisation distortion, i.e. the difference between the original wave and the reconstructed wave, see Figure 9. The quantiser, i.e. the circuit that takes the samples and compares them with the levels we have chosen as reference points, selects the nearest reference point. For example, sample A is closer to the higher reference level, so this is selected. Sample B is closer to the lower

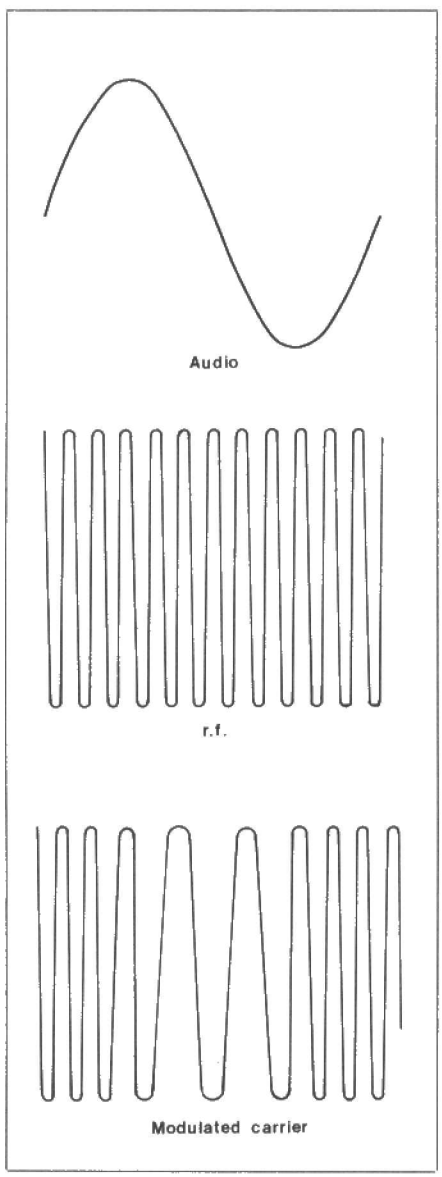


Figure 2. Frequency Modulation

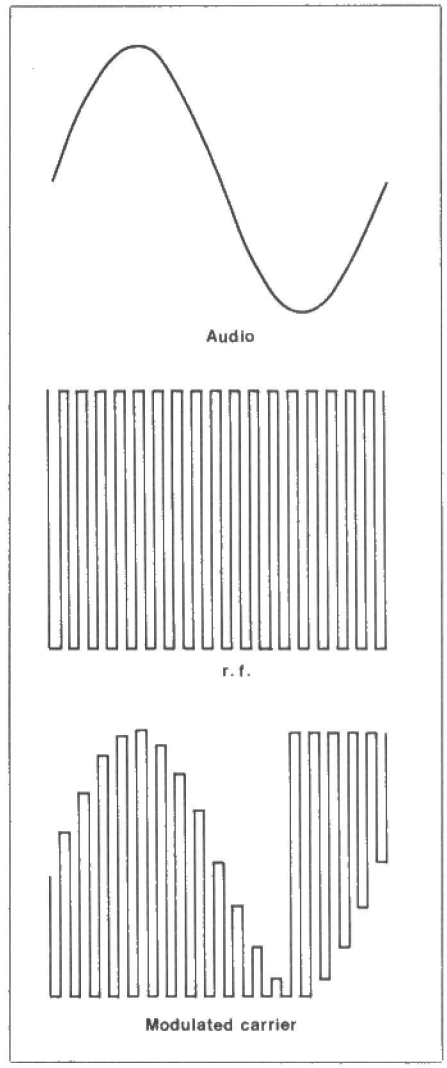


Figure 3. Pulse Amplitude Modulation

of the reference levels so the lower one is selected. Straightaway, we can see that the reconstructed waveform is not going to be the same as the original.

So how many samples per second does one take? If we take too many, we are transmitting unnecessary information. If we take too few, the reconstructed wave does not resemble the original. In practice, the sampling rate needs to be twice the highest frequency one hopes to transmit. If we take a telephone channel 4kHz wide, the frequency band allocated to speech is 300Hz to 3.4kHz. Those with squeaky voices will have additional frequencies higher than 3.4kHz but most of the power and the frequencies for intelligible speech lie in this band, see Figure 10. Allowing for filter cut-off, gives a band of 4kHz. If the highest frequency to be transmitted is 4kHz, the sampling rate needs to be 8kHz. The reason for choosing a sampling rate that is at leave twice the highest frequency can be seen in Figure 11. Choosing a sampling rate of 6kHz causes the lower sideband to overlap with the audio band being sampled, thus giving distorted sampling. The quantisation discussed above is called 'Linear Quantisation', i.e. the reference steps are of equal height. Noise in a communications channel is fairly constant, so it would have little effect on high amplitude speech, but the signal to noise ratio

would be poor for low amplitude speech. To overcome this, a non-linear quantiser is used (say a curve with a logarithmic law) to give greater emphasis to low level signals. It does this by assigning more reference levels to low amplitude signals and therefore fewer to high amplitude signals, see Figure 12. The overall effect is to compress the signal so in fact, a signal compressor could be used followed by a linear quantiser. If a compressor is used at the transmitting end, an expander must be used at the receiving end; therefore, the word 'compander' (compressor-expander) will often be heard in association with PCM systems. Using digital techniques of this type, low level signals in the presence of noise have been recovered during space missions.

One type of compander that is used has a curve as shown in Figure 13a. This curve is nearly logarithmic and it can be seen that the maximum advantage occurs at the lower levels. From Figure 13b, for an input signal of one step, an output of sixteen steps is obtained. Therefore, the companding advantage is:-

$$20 \log \left(\frac{16 \text{ steps}}{1 \text{ step}}\right) = 20 \log 16 = 24\text{dB}$$

The next largest advantage occurs at an input between step one and two where the advantage is 18dB.

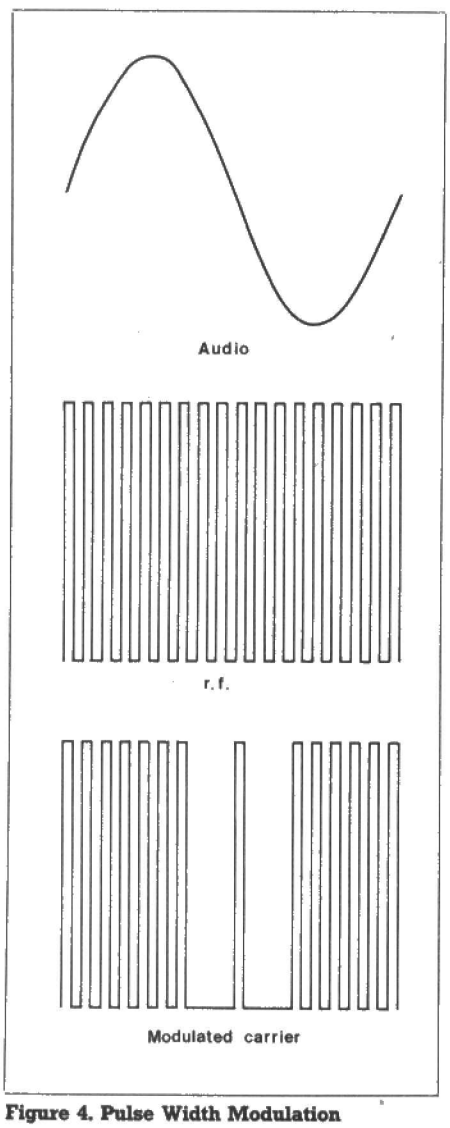


Figure 4. Pulse Width Modulation

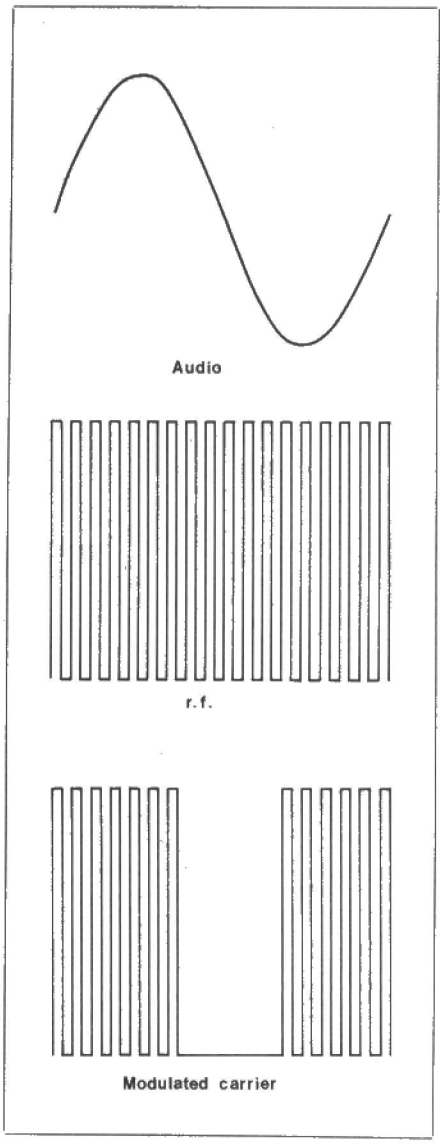


Figure 5. Pulse Position Modulation

Time Division Multiplex

Since the sampling pulses are of such short time durations, of the order of a few microseconds, several speech channels can be transmitted at once. This is achieved as in Figure 14. The first sample of channel one is transmitted followed by the first sample of channel two and so on till the last channel. Then the second sample of channel one, the second sample of channel two, till the last channel. And so on till all the samples have been transmitted and the switch returns to the first sample of the first channel. Of course, some means must be found of synchronising the receive switch with the transmit switch so that the same sequence of digits is received as was transmitted. Otherwise you will find yourself talking to auntie Flo instead of the President of the United States. Or is it the other way round?

This is the principle of time division multiplex. Each channel is chopped up into time windows and these time slots are interleaved so that they can be transmitted as a pulse train down a single link between two stations, Figure 15.

PCM Systems in Use

At present, the systems in use are the UK 24 channel system, the US 24 channel system and the newer European standard 30 channel system. The UK has some 7000 24-channel systems using a logarithmic law (A-law) and 7 bits to describe each sample, therefore 128 quantisation levels can be used (2^7 = 128). The gross digit rate is given by multiplying the number of channels by the sample rate and the bits per sample. If the number of channels is 24, the sampling rate is 8kHz and the bits per sample are 8 (the 7 above plus an extra one for signalling, synchronisation or spare), then:–

$$24 \times 8000 \times 8 = 1.536 \text{ Mbit/s}$$

The American system uses μ (Greek letter mu) law encoding with 100 levels and a gross bit rate of 1.544 Mbit/s.

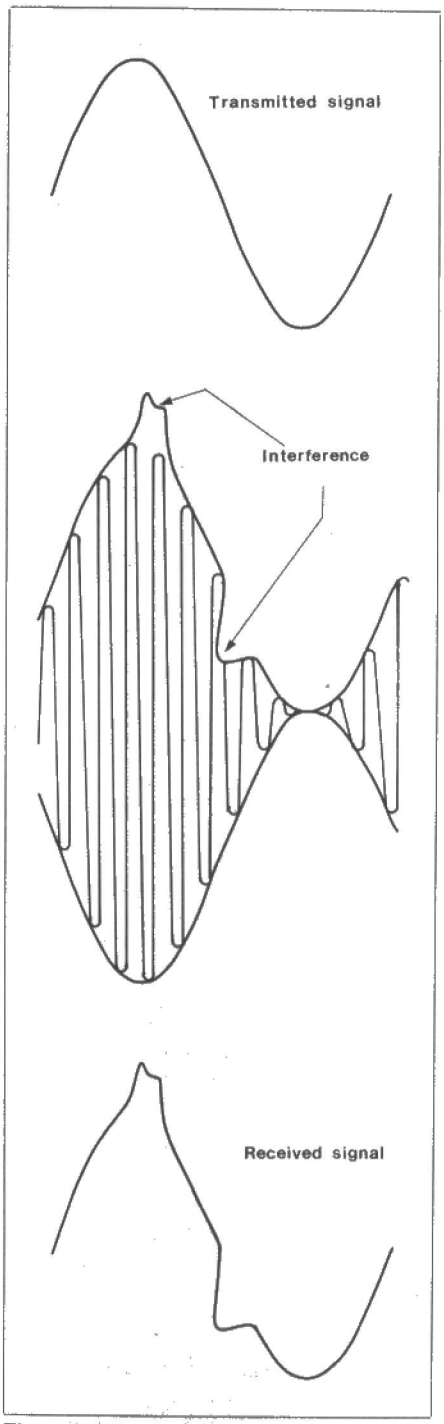


Figure 6. Noise Interference

Actually 1.536 Mbit/s plus the S bit in time slot 24 for synchronisation giving an overall rate of 1.544 Mbit/s.

The European 30 channel standard uses 8 bits per sample giving 256 quantisation levels (2^8). This gives a more faithful reproduction of the waveform since more levels are being sampled. This is very important in the new era of digital transmission since several links can be placed in tandem and several analogue to digital conversions can take place without degrading the signal. The gross digit rate is 2.048 Mbit/s and in the digital network this basic 2 Mbit/s block will be combined with others to give hierarchies of 8 Mbit/s, 34 Mbit/s and 140 Mbit/s. That is why 30 channel PCM is so important. Table 1 summarises some of the above points.

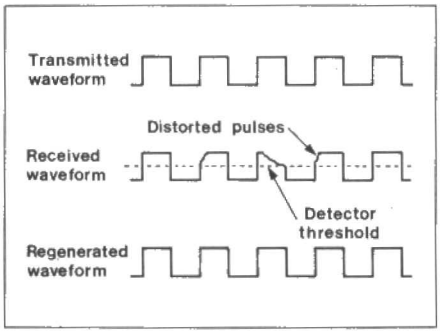


Figure 7. Regenerating Pulses

The choice of whether to use audio cables (pairs of copper wire) or frequency division multiplex (FDM) on coaxial cable or to use PCM depends on the cost of the terminal equipment and the distance between terminals. Figure 16 shows the comparative costs of audio transmission, FDM and PCM. It can be seen that PCM is economical for distances between 12km and 38km approximately.

The UK 24 Channel PCM System

Why 24 channels? Because the audio pairs of copper conductors in the cities are capable of supporting the maximum bandwidth required by such systems. If larger bandwidths are required, one has

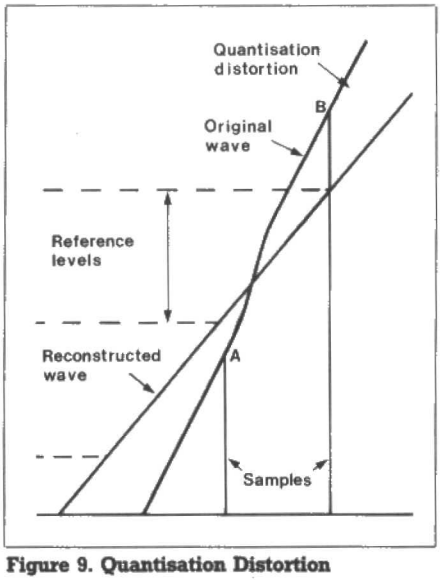


Figure 9. Quantisation Distortion

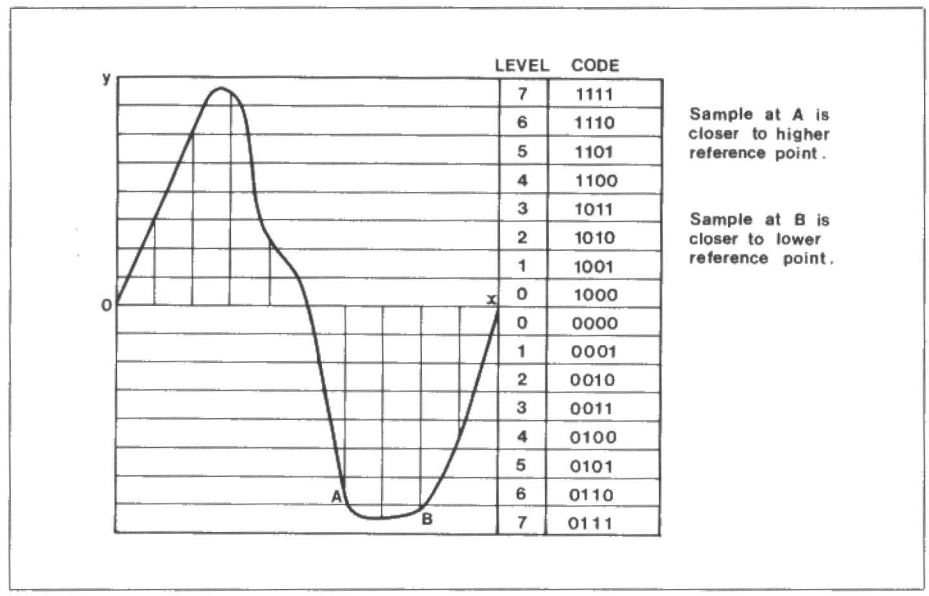


Figure 8. Linear Quantisation

to use coaxial cable, optical fibre or use any of the multitude of codes for compressing digital signals. The last method makes the terminal expensive. Even without digital compression, if the audio cables in a city are all utilised, the choice is either to run a new cable or use PCM. A new cable is cheaper but if there is no more room in the duct then PCM has to be used.

Figure 17 gives the frame structure of the 24 channel PCM system. A

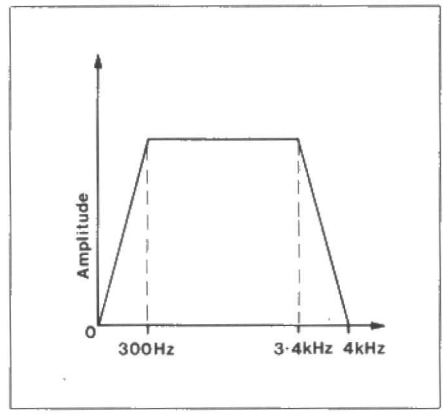


Figure 10. Telephone Channel

sampling rate of 8kHz means that a channel is sampled once every 125μs. This is called a frame which holds a sample of each of the 24 channels. Therefore, a time slot is 125/24 = 5.2μs. And eight bits are used to describe each time slot, therefore each bit is 5.2/8 = 0.65μs wide. In practice a 50% duty cycle is used so these pulses are only 0.32μs wide. This 50% duty cycle gives the regenerators along the route the maximum opportunity for detecting a pulse without confusing one pulse with its neighbour. On the other hand, one does not want to make the pulses too narrow since f = 1/T, i.e. the bandwidth increases.

Four of the frames in Figure 17 makes a multiframe (500μs). The equipment uses clocks of 8kHz for sampling and 1.536MHz for transmitting the signal to line. Power for transmission is 50mA, 75-0-75 volts. The pulse train of Figure 17 undergoes two processes, alternate digit inversion (ADI) and alternate mark inversion (AMI), Figure 18. It undergoes ADI first. Every alternate digit is changed to its opposite, i.e. one is changed to zero and if there is a zero it is changed to one. The idea is to give a higher density of marks (ones) so that a regenerator can extract timing information. More than eight consecutive zeros would impair the timing information and a string of fifteen zeros would make the regenerator run down and stop.

A unipolar pulse train has a DC component and conductors would have to be much thicker in order to transmit direct current. This is overcome by inverting every alternate mark giving a bipolar pulse that is finally transmitted to line. A simple block diagram of a transmit and receive system is shown in Figure 19. The low pass filter is for removing noise. Note the symbol for a regenerator. Regenerators are placed about every 2000 yards and provided there are less than ten pairs of regenerators, end to end, power feeding can take place. If a route is longer, a power feed turn round arrangement is adopted as in Figure 20 and intermediate power feeds used.

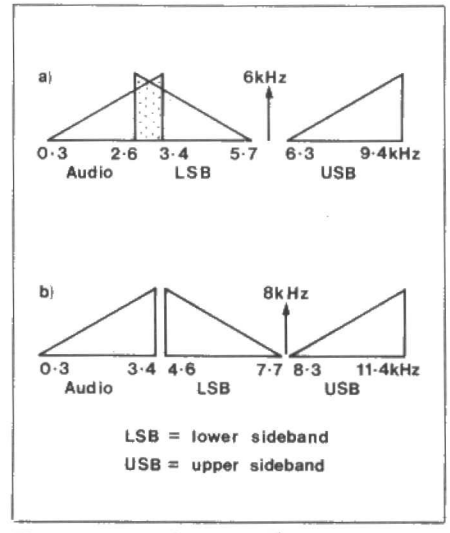


Figure 11. Sampling at 6kHz and 8kHz

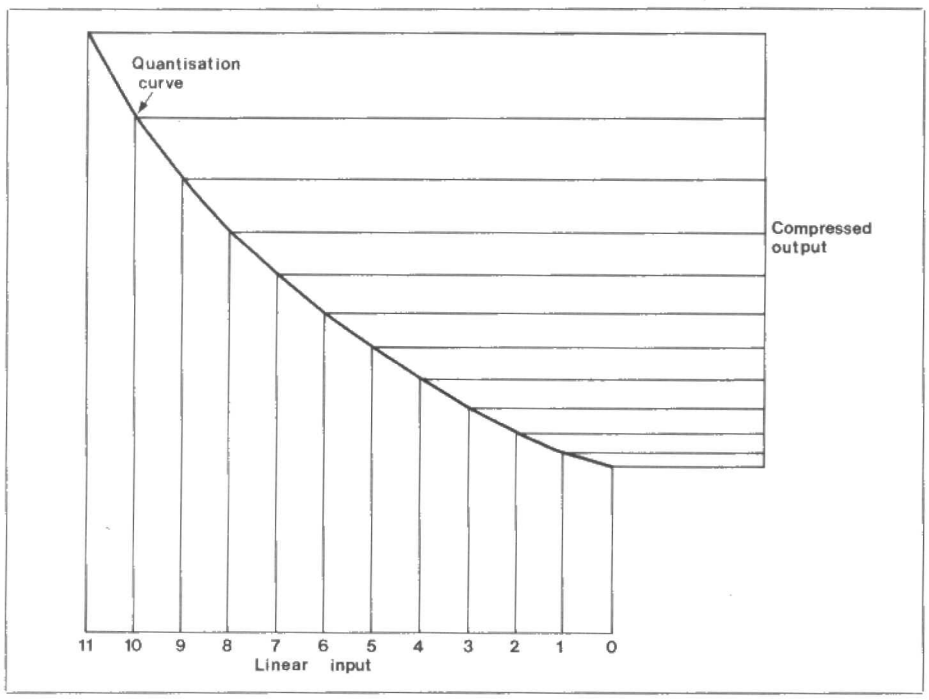


Figure 12. Non-linear Quantiser

Encoders and Decoders

Figure 21 shows how an encoder is implemented. The incoming signal has to be sampled and the value held. This is achieved by gates G1 and G2. Capacitor C is charged up and discharges via G1. It is then ready to charge up with the next value of current. The polarity of the signal determines whether the first digit will be a 1 or 0 and the comparator decides this. The remaining digits are derived by successive subtraction and comparing with standard currents generated by attenuators. As an example, Table 2 shows how the last four digits are derived given that the residual current is 1.3. If the test current is less than the residue, a one is allocated and if it is greater than the residue, a zero is mapped. The final residue of 0.075 is the quantisation error.

Figure 22 shows a decoder where the process is reversed and once again by comparison with current attenuators, a reconstituted PAM signal is obtained. Firstly of course, the incoming serial bit stream needs to be converted to a parallel stream.

Repeaters

A repeater arrangement is shown in Figure 23, and the waveforms in Figure 24. The clean bipolar pulse that was transmitted has become attenuated and

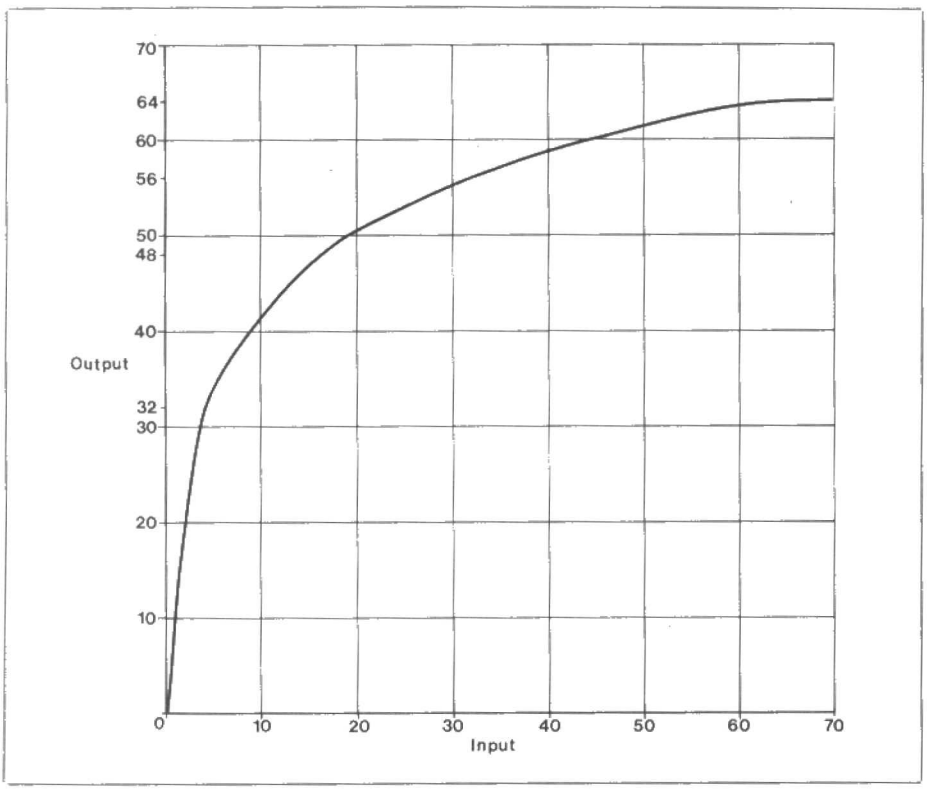


Figure 13(a). Near Logarithmic Curve

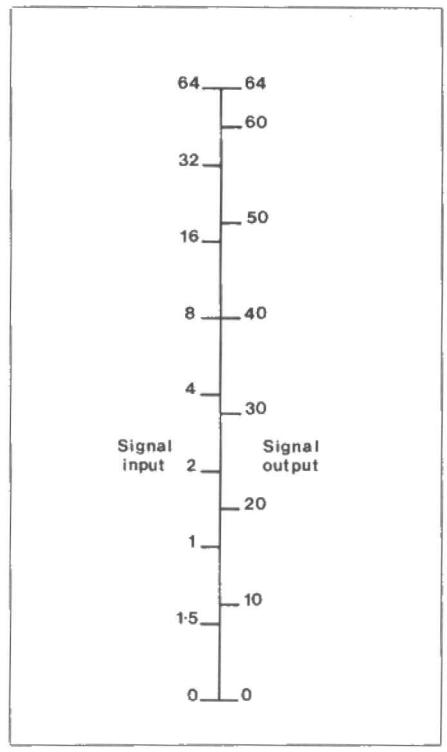


Figure 13(b). A-Log Scale

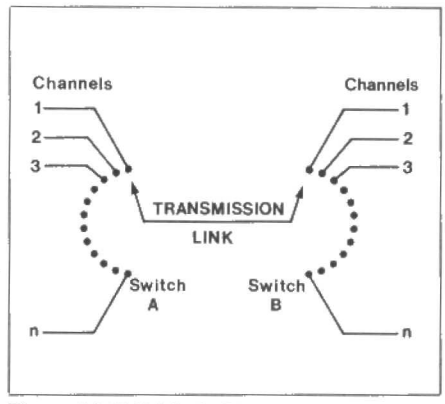


Figure 14. TDM Switching

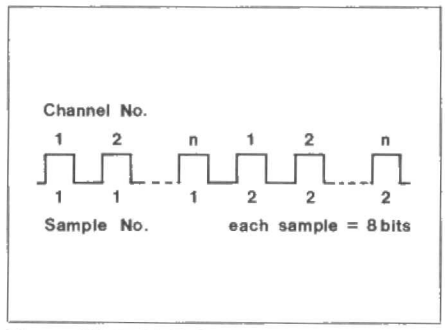


Figure 15. TDM Pulse Train

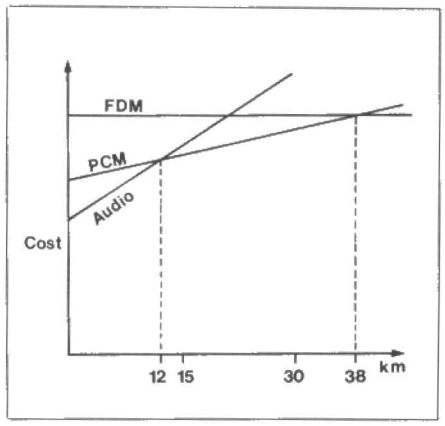


Figure 16. Comparative Costs

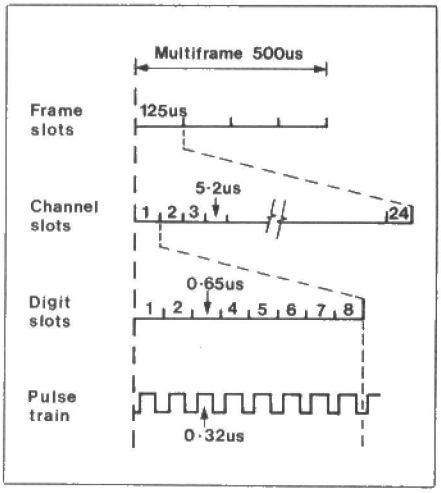


Figure 17. 24 Channel Structure

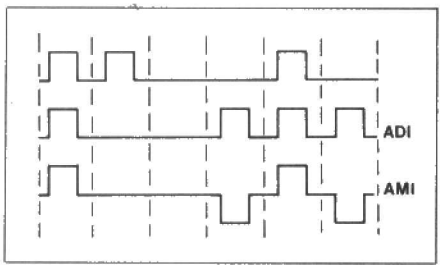


Figure 18. ADI and AMI

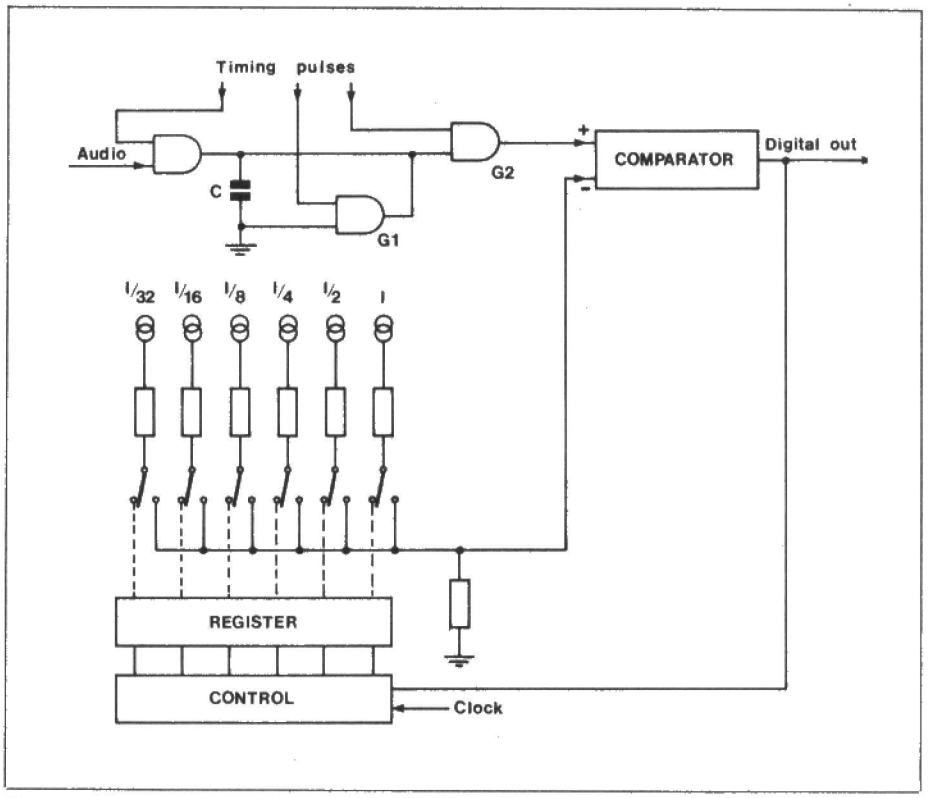


Figure 21. Encoder

turned into a ragged analogue shape. The equaliser turns the barely recognisable humps into little peaks which can be amplified and squared. The square pulse is then differentiated to provide timing spikes and the final clean bipolar pulse transmitted to the next repeater. A block diagram for a transmit/receive terminal is shown in Figure 25.

Alarms and Maintenance

Alarms on the transmit/receive multiplex terminal indicate loss of synchronisation or power or high error rates. When channel 12 is not in use, it carries a 2kHz tone for checking the coder and decoder. This is called 'Codec Monitoring'. When a regenerator (repeater) fails, the method of locating the position of transmitted has become attenuated and the faulty regenerator is the trio method, Figure 26. Sets of three pulses, two positive going and one negative going or two negative going and one positive going, are sent in groups as shown. The resulting DC level is filtered to give an audio signal and each repeater has a distinct bandpass filter to pass a pre-alocated frequency. Therefore the repeater that fails to return its identification signal is the faulty one.

It is also possible to detect an ageing regenerator before it has failed. This is done by increasing the density of the trios without altering the audio frequency. The signal generator has a switch for selecting trio densities from 1 in 4 (3 positive, 1 negative) to 1 in 11. This effectively increases the DC bias and the curve of an ageing regenerator can be seen in Figure 27.

30 Channel PCM

The European 30 channel PCM system will also be adopted by the UK and will be the fundamental building block of digital hierachies. The 30 channel system does not have any drastically new ideas. It is really only a tidy up of the 24 channel format. For instance, signalling in the 30 channel format is bunched in time slot 16 instead of being spread out. Similarly the frame alignment signal is bunched in time slot 0. Table 3 compares the two systems. A greater number of regenerators can fit in a repeater case for the 30 channel system. This is a tribute to microtechnology. Manufacturers are even talking of spectacular reductions on the

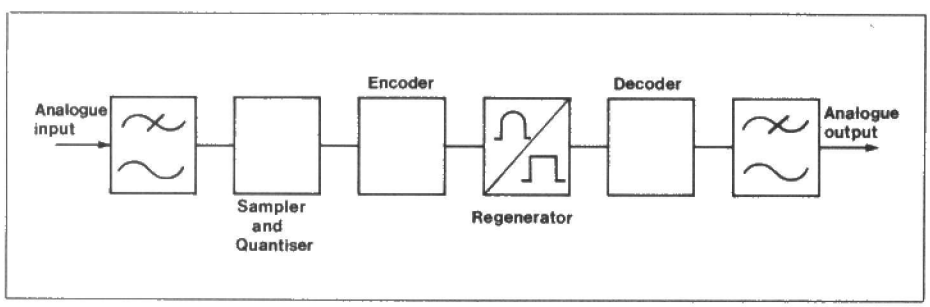


Figure 19. Transmit/Receive System

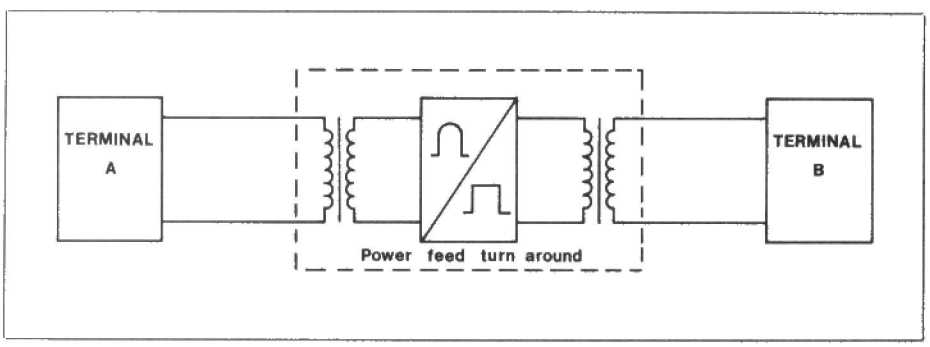


Figure 20. Power Feeding Arrangements

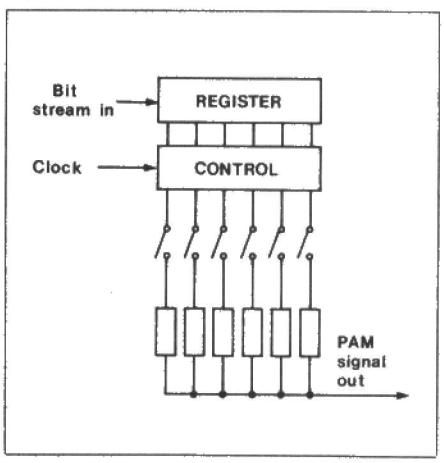


Figure 22. Decoder

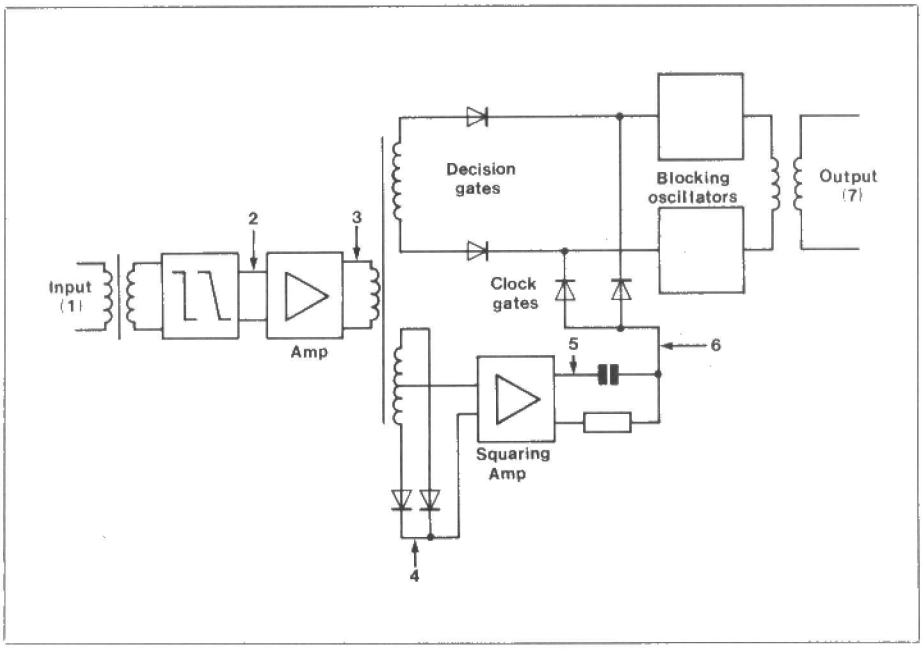


Figure 23. Regenerator

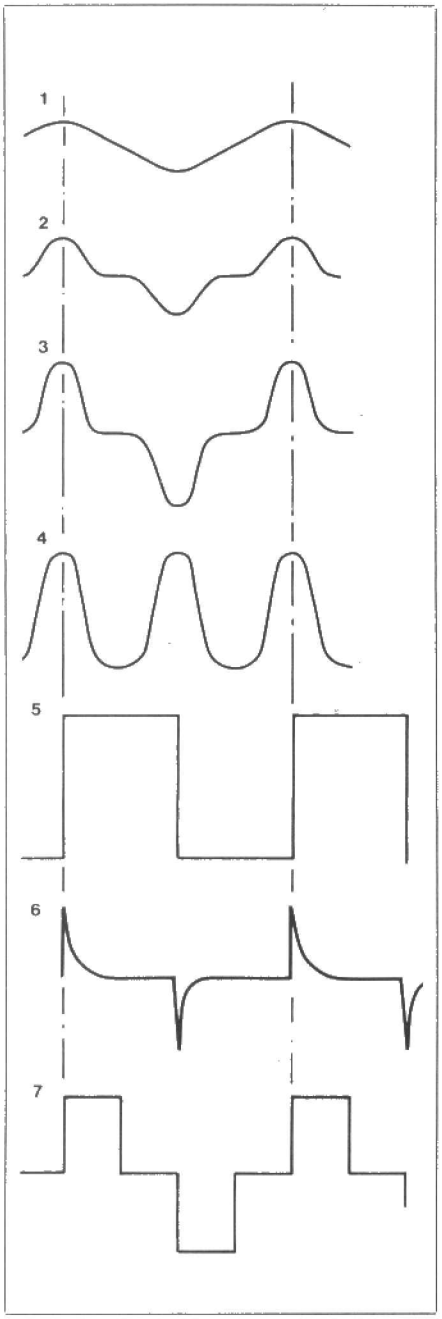


Figure 24. Waveforms for Figure 23.

multiplex racks. Racks that used to house 20 systems will soon house 80 systems.

Table 3 also shows that 16 systems can be put in tandem since the 30 channel system uses 256 quantising levels to describe an audio signal more faithfully than the 24 channel system. As before, A-law companding is used. If a linear law were used, 12 bits would be required instead of 8 bits to describe the signal amplitude satisfactorily in the presence of noise. Eventually, 30 channel PCM will operate over optical fibre but at present, there is a lot of 'paper core quad trunk' (PCQT) cable with 0.63mm conductors in the UK network and these will be utilised.

30 Channel PCM Frame Format

Since two extra time slots are required for signalling (time slot 16) and frame alignment (time slot 0) plus 30 more for the channels, this is a total of 32 time slots. A sampling rate of 8kHz and 8 bits per sample gives a gross digit rate of 8000 x 32 x 8 = 2.048 Mbit/s. A frame contains a sample of all the channels and is 125μs wide, see Figure 28. A multiframe consists of 16 frames and is repeated every 2ms. Each time slot is 125/32 = 3.9μs. There are 8 bits per time slot; therefore each pulse would be 3.9/8 = 488ns, but at a 50% duty cycle, this is reduced to 244ns.

As in Figure 25, the frame alignment and signalling information is added to the bit stream after the speech signals have been processed. The signalling information consists of the telephone number being called and duration of the call. The composite signal then undergoes alternate digit inversion but instead of alternate mark as the next process, it is coded in high density bipolar 3 (HDB3). This HDB3 code has the same effect as AMI in preventing too many zeros. It does in fact, restrict the number of zeros to 3. When any group of 4 zeros is encountered, the last one is changed to a mark of the same polarity as the previous mark, Figure 29. This is called a 'Violation' (V) since it upsets the DC balance and if there are an even number of marks or there is no mark between each voilation, then a substituted mark(s) is inserted in place of the first of the four zeros. The polarity of the substituted mark is opposite to that of the previous mark.

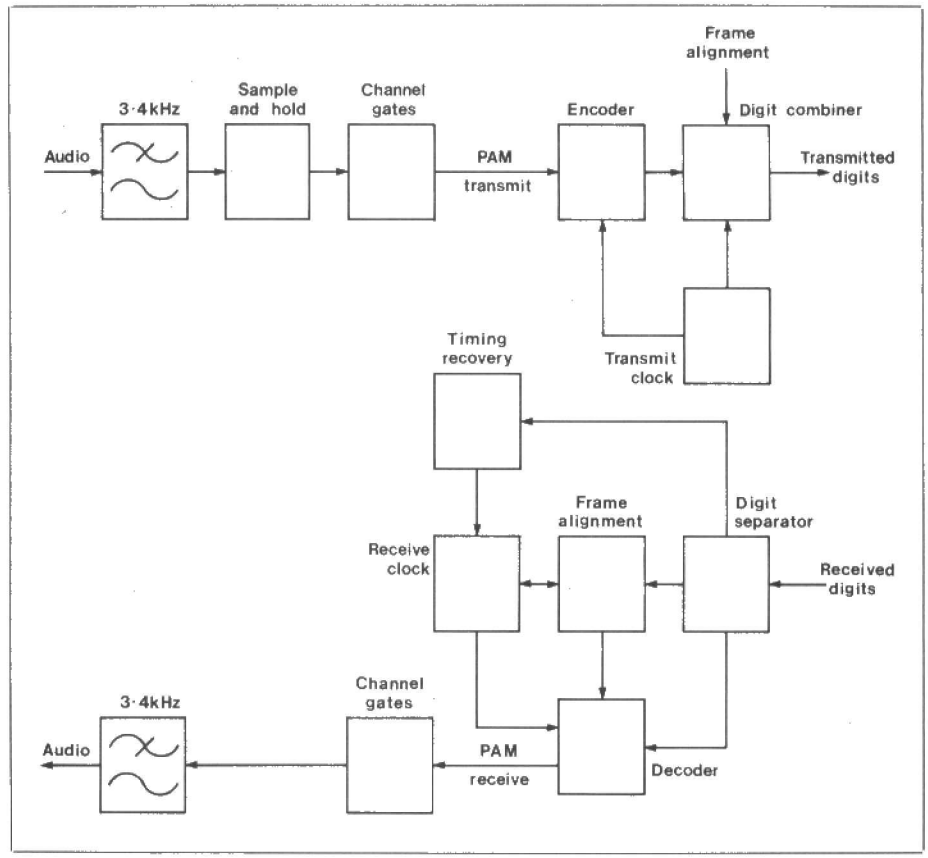


Figure 25. Transmit/Receive Terminal

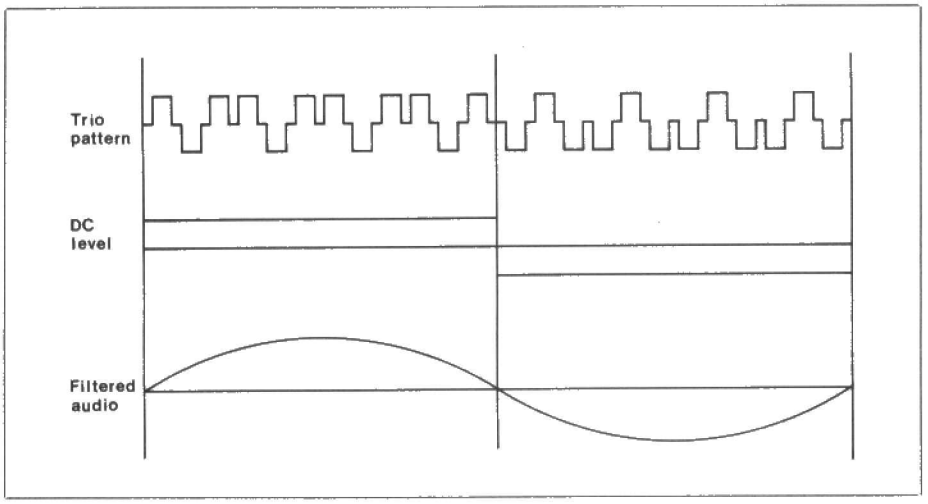


Figure 26. Trio Testing

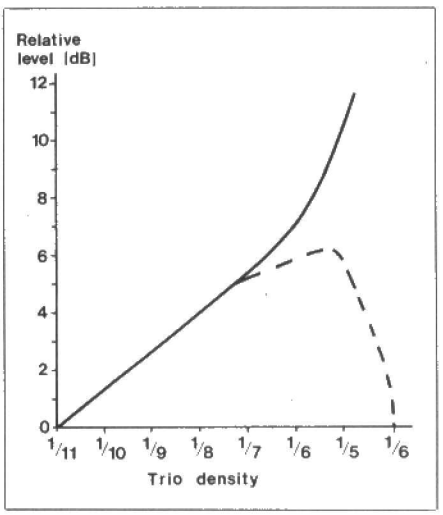


Figure 27. Ageing Regenerator

General Features of 30 Channel PCM

The PCQT cable mentioned earlier comes in 13 sizes, from 14 pairs to 1040 pairs. Not all pairs can be used because of cross talk but with careful choice, the use can be maximised. In a 504 pair cable, about 144 pairs can be used.

A repeater is a general term for equipment that amplifies a signal and sends it on. The term is used loosely for analogue and digital signals. However, the term regenerator is more appropriate in a digital environment since a regenerator replaces old pulses with new. For lightning protection, zener diodes are used on regenerators, this is shown in Figure 30. Jitter is a problem encountered in digital systems. Jitter is defined as short term variations in a pulse position, see Figure 31. To prevent this, the equalisation must be good and the spikes for timing information accurate. A regenerator consumes about 350mW and, as before, the power to line is 50mA, 75-0-75 volts.

Techniques Closely Related to PCM

Associated with PCM are a number of techniques under the title of Digital

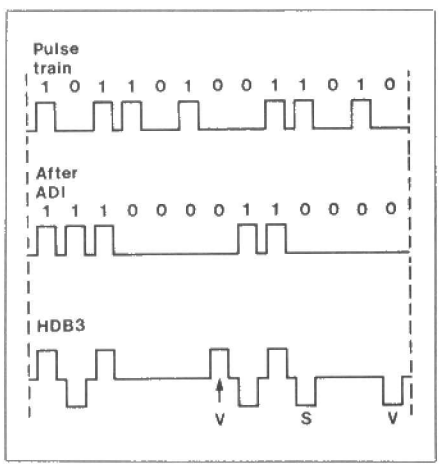


Figure 29. HDB3

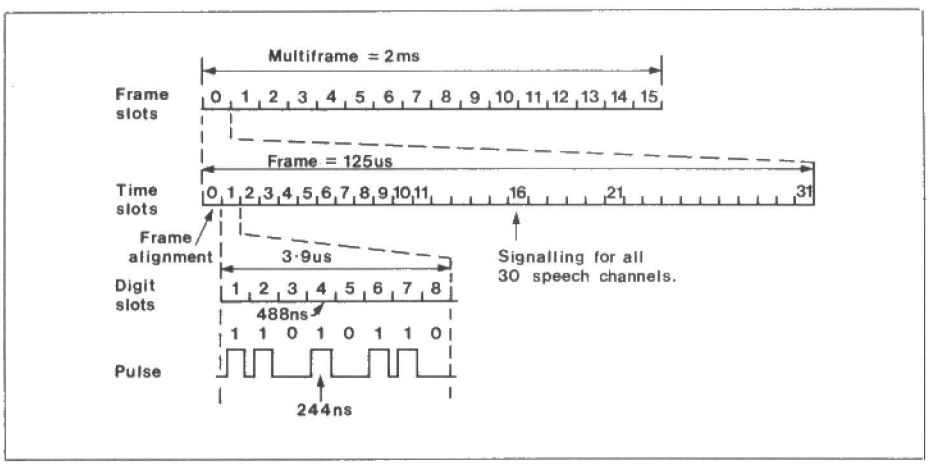

Multiframe = 2ms
Frame slots
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Frame = 125us
Time slots
0 1 2 3 4 5 6 7 8 9 10 11 16 21 31
Frame alignment
3·9us
Signalling for all 30 speech channels.
Digit slots
1 2 3 4 5 6 7 8
488ns
1 1 0 1 0 1 1 0
Pulse
244ns

Figure 28. 30 Channel Format

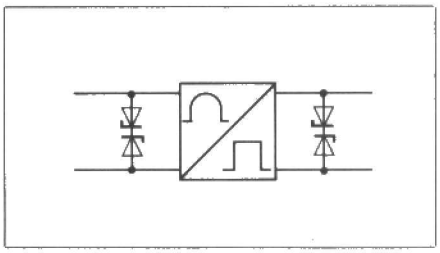


Figure 30. Lightning Protection

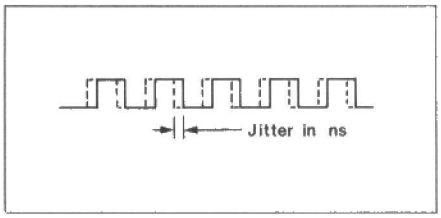


Figure 31. Jitter

Speech Processing (DSP). These include Low Rate Encoding (LRE) and Digital Circuit Multiplication Systems (DCMS). The whole idea of DSP is to get away with as much as possible by paying as little as possible. Sounds like human nature. These techniques will be dealt with briefly. Another item of interest is Time Division Multiple Access (TDMA), for satellite working. This is only an extension of the TDM idea for PCM, where each channel gets attention for a fixed time slot. Using TDMA, each country accesses a satellite for a short burst within a 2ms frame. The old method was Frequency Division Multiplex (FDM). But instead of allocating bandwidths as in FDM, TDMA allocates time.

Digital Speech Processing

If two people are holding a conversation, one speaks and the other listens. Therefore, there is a 50% redundancy straightaway and only one path is required instead of two, Figure 32. Taking pauses into account, the usage is as low as 40%. A computer is fast enough to snatch the free path and allocate it to another talker. To avoid any clipping of speech, a delay line and buffer are introduced. Various generations of such equipment have been in use since the 1960s under such general names as Time Assigned Speech Interpolation (TASI) and Circuit Multiplication Equipment

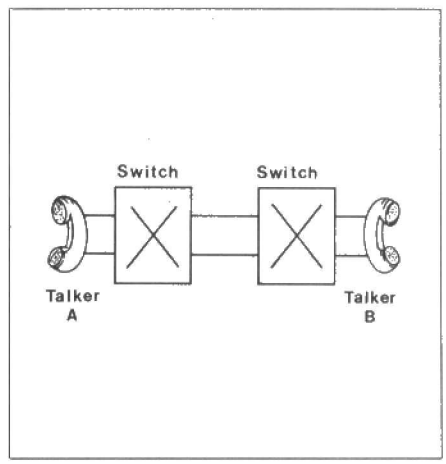


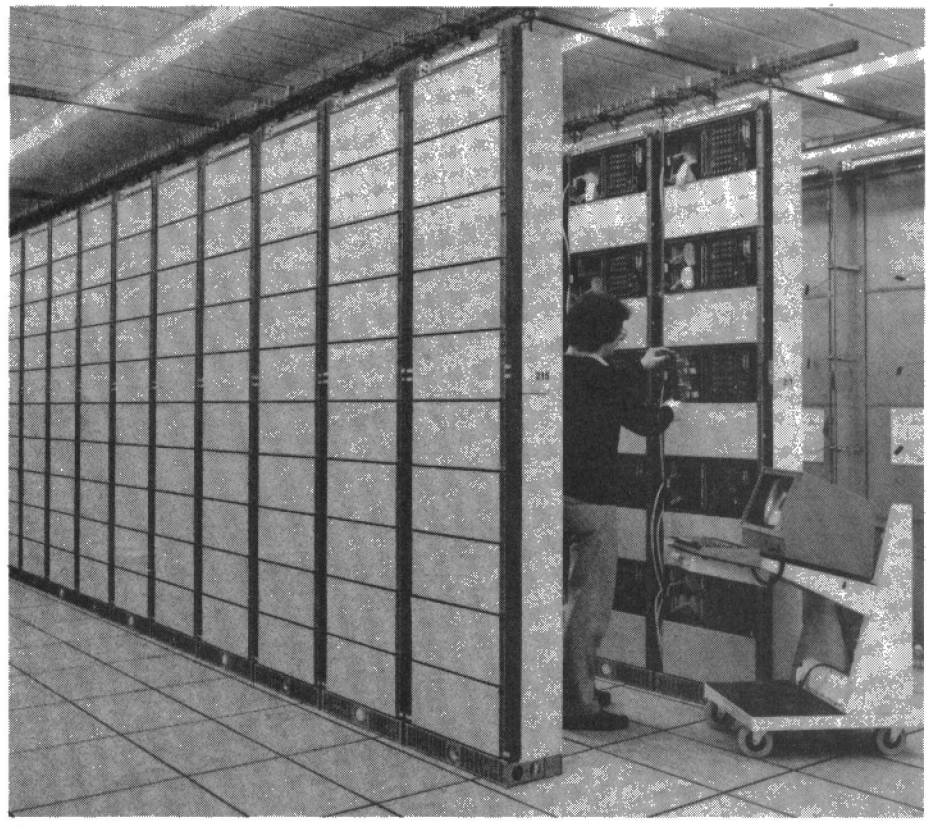
Figure 32. Redundant Speech Path

(CME). At the present time, although the computer processing is digital, the speech is analogue. A generic name like CME is self explanatory, it effectively increases the number of circuits available by continuously re-allocating vacant ones on a demand basis. The above equipment varies in size from 31 derived circuits on 16 actual circuits to 240 derived on 120 actual circuits or bearers. We can see that 31/16 or 240/120 gives roughly a 2:1 ratio, i.e. the 50% redundancy we discussed earlier.

In the digital era, when speech is converted to a bit stream the terms Digital Speech Interpolation (DSI) and Digital Circuit Multiplication Systems (DCMS) will be more commonly used.

Low Rate Encoding

Another method of reducing the number of bits and hence reduce the required bandwidth is to use fewer than 8 bits for encoding. At present 64kbit/s is required to encode a 4kHz speech channel (1.536Mbit/s / 24 channels = 64kbit/s) using various coding techniques this 64kbit/s can be reduced to 32kbit/s, 16kbit/s and even 8kbit/s. The quality of speech suffers at the lower rates. Using 4 bits per sample instead of 8 bits, the bit rate is reduced from 64kbit/s to 32kbit/s and the speech quality is acceptable. This gives a 2:1 'advantage', i.e. we can have 2 speech channels transmitted in the same time frame as it took to transmit one channel formerly. If this 2:1 advantage is combined with the 2:1 advantage of digital speech interpolation, we get a 4:1 advantage. These digital coding techniques were never possible before with analogue signals. Of course, the hardware costs go up but who cares, with the cost of very large scale integration coming down, there will soon be purpose built chips for speech processing. Some of the commonly used techniques will be described below.



Photograph supplied by STC Ltd.

STC 30-channel primary multiplex being installed into an international digital switching system

System	Number of Quantisation Level	Sampling Law	Bits per Sample	Gross bit rate (Mbit/s)
UK 24 channel	128	A Law	7	1.536
USA 24 channel	100	μ Law	7	1.544
European 30 channel	256	A Law	8	2.048

Table 1. General Comparison of PCM Systems

Attenuator Number	Digit Number	Test Current	Residue	Test current greater than residue	Test current less than residue	Bit allocated
5	5	1	1.3		×	1
6	6	0.5	0.3	×		0
7	7	0.25	0.3		×	1
8	8	0.125	0.05	×		0
			0.075	*(final residue)*		

Table 2. Encoding Process

Feature	24 Channel	30 Channel
Time slot	5.2μs	3.9μs
Pulse width	320ns	244ns
Multiframe	4 frames	16 frames
Encoding bits	7	8
Gross bit rate	1.536Mbit/s	2.048Mbit/s
Line code	AMI	HDB3
Signalling	Distributed	Time slot 16
Frame alignment	Distributed time slots 9 to 24	Time slot 0
Codec monitoring	2kHz tone on channel 12	Locally during time slot 0
Maximum number of systems in tandem	4	16
Regenerators in one case	24	36
Error detection	Bipolar violations in AMI stream	Errors in frame alignment signal

Table 3. Comparison of PCM Formats

Delta Modulation

Instead of sampling the waveform regularly, one bit can be reserved to say if the signal amplitude is increasing or decreasing since the previous sample. This is called 1-bit delta modulation. The disadvantage is that if it takes a step in the wrong direction, it retains the error and any subsequent errors. Therefore, it needs to be reset at regular intervals.The result can be seen in Figure 33. The signal to noise ratio also depends on the size of the step. Slope overload occurs for small steps and granular noise for large steps. Granular noise is so called because this technique, when used to code a television picture, shows up the grain. A slightly more sophisticated form of delta modulation is adaptive differential PCM (ADPCM) in which the step size can be varied according to the dynamic range of the input signal.

Nearly Instantaneous Companding (NIC)

A non-linear compander is used as before, and blocks of samples examined to arrive at the maximum sample value. This maximum value then determines the slope of coding. Low signal levels may need different coding slopes. One type of programme equipment (NICAM 3) converts the audio band, 40Hz to 15kHz, into a 338kbit/s stream.

Continuously Variable Slope Delta Modulation (CVSD)

All coding systems operate on the speech envelope in one way or another. For instance, low frequencies in speech occur in a longer time frame than high frequencies. Therefore, fewer bits are required to describe low frequency components. The CVSD method feeds the speech band (300 to 3400Hz) and the speech envelope to a 1-bit delta modulator. The speech envelope is fed through a low pass filter of 100Hz so that it does not interfere with the speech. This envelope is then used to change the step size slowly with a time constant of 10ms. In other adaptive modulation techniques, the step size is changed on successive samples, depending on consecutive ones and noughts in a row. This is an indication of the rate of change of the input signal. But CVSD adapts the step size slowly depending on the average number of ones in the 10ms frame. Chips for CVSD encoding like the Motorola MC3418 are already available.

Sub-band Coding

In this method, a row of bandpass filters divides the speech band into four to eight sub-bands. These sub-bands are then modulated so that each band starts at zero frequency. Then each band is sampled at the Nyquist rate (twice the highest frequency). The total number of samples presented for encoding remain the same as for a 4kHz band sampled at 8kHz. For instance, if there are four sub-bands each of 1kHz, they would each be sampled at 2kHz. At the received terminal, the sub-bands are decoded and modulated again to give them their rightful places in the 4kHz spectrum.

So where is the advantage in all this black magic? The advantage lies in being able to allocate more bits to the lower frequency band since the ear is more sensitive to noise at the lower frequencies. Also quantisation noise in each band is confined to that band and is prevented from masking speech in another band. Signal processing of such a complex nature would be unthinkable if it had not been for the low cost of chips.

Conclusions

Starting with pulse code modulation as a basic technique for digitising speech, the 24 channel and 30 channel formats were described. However, digital transmission is wasteful in bandwidth compared to analogue transmission and modern technology rises to the challenge of reducing this bandwidth. Some of the more common methods of bandwidth compression have been outlined above. There are many others but I hope this article has given a flavour of some of the more commonly used techniques.

The common theme of all these methods is to describe or predict the speech envelope as accurately and economically as possible. Therefore, such methods are not restricted to speech, but can be used equally well for any other analogue waveform, e.g. television. For speech coding, designers are already making claims of 16kbit/s and even 8kbit/s. As for every limbo dancer, the challenge seems to be , "How low can you go!"

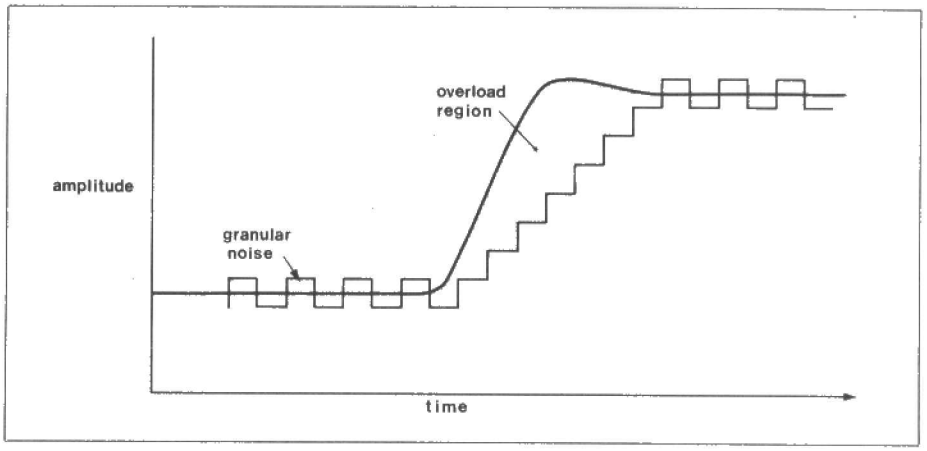
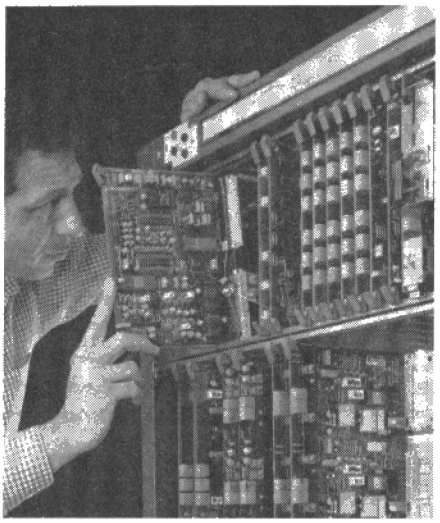


Figure 33. Delta Modulation



30 telephone channels in a 2048 kbit/s stream

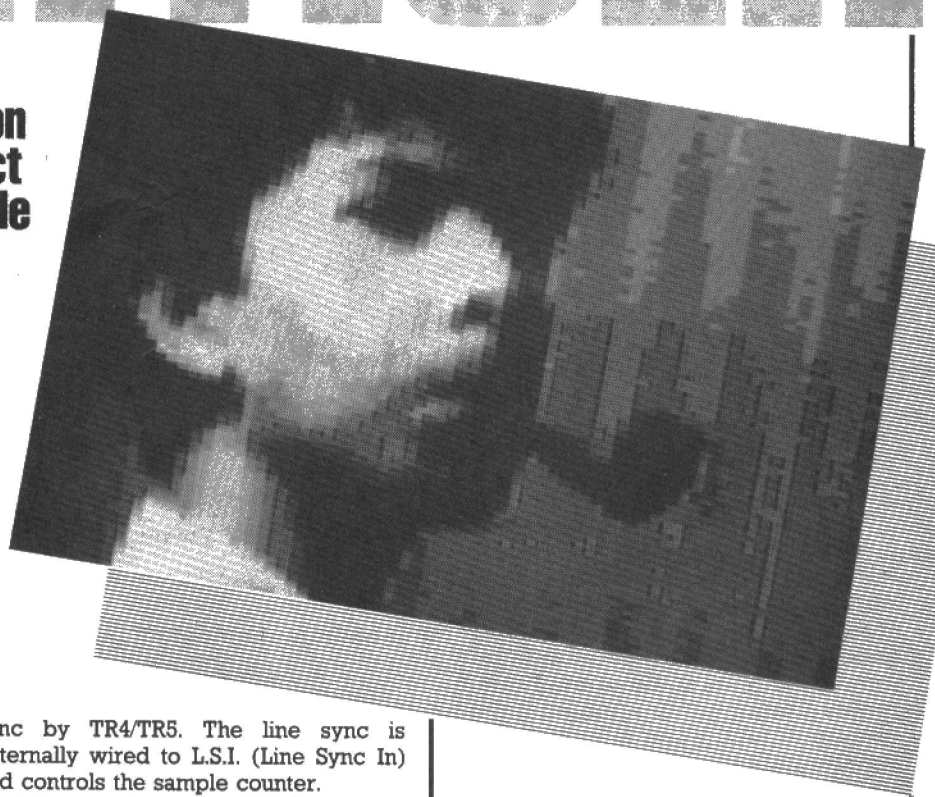
Glossary of Terms

ADI	Alternate Digit Inversion.
ADPCM	Adaptive Differential Pulse Code Modulation.
AMI	Alternate Mark Inversion.
Compressor	Circuit to compress a frequency band.
Compander	Compressor and expander.
CME	Circuit Multiplication Equipment.
CVS	Continuously Variable Slope.
DSI	Digital Speech Interpolation.
DCMS	Digital Circuit Multiplication Systems.
DSP	Digital Speech Processing.
Expander	Circuit to reverse the compression process.
FDM	Frequency Division Multiplex.
Frame	One sample of all the channels.
HDB3	High Density Bipolar 3.
Jitter	Short term variation in a pulse position.
LRE	Low Rate Encoding.
NIC	Near Instantaneous Companding.
PAM	Pulse Amplitude Modulation.
PCQT	Paper Core Quad Trunk.
PPM	Pulse Position Modulation.
PWM	Pulse Width Modulation.
Quantisation	Process of deciding which reference level is closer to a wave form sample.
Quantisation distortion	Difference between original wave and reconstructed waveform.
Sampling	Process of taking amplitude values of a wave at pre-determined intervals.
TASI	Time Assigned Speech Interpolation.
TDM	Time Division Multiplex.
TDMA	Time Division Multiple Access.
Time slot	Sample of one channel.

Video DIGITISER

★ Resolution 312 x 255
★ 8-bit Luminance Resolution
★ Controller Board to detect Line & Synch Pulses Available

by Mark Brighton and Robert Kirsch



A Video Digitiser is a device which converts a video picture, such as the output of a video camera or V.C.R. (still frame) into digital words representing the luminance or brightness of co-ordinates (X, Y) within the picture. Thus, by sampling and converting all co-ordinates in turn, a stream of digital words representing the video picture may be sent to a host microcomputer and displayed on a graphics screen, or stored on disk or tape.

The resolution of the final computer picture will depend on the graphic capability of the host computer, up to the limits of the Digitiser.

In this case, the maximum vertical resolution of the Digitiser is the same as the number of complete lines in a video frame, i.e. 312 (although twice this number should be available if the interlace frame is also stored).

The horiztonal resolution is 255 which is the possible number of sample points in one line scan, although some of these will be in non-valid picture area.

The resolution of the luminance samples is 8-bit for a standard video level, ≃ 1 volt of video. Most micro-computers will not be able to combine these resolutions in a graphic screen, and a compromise between (X, Y) resolution and luminance resolution will have to be made when programming.

Circuit Description

In Figure 1, the video content of the incoming signal is stripped off by TR1 to leave composite sync, which is further split into frame sync by TR2/TR3 and line sync by TR4/TR5. The line sync is externally wired to L.S.I. (Line Sync In) and controls the sample counter.

The sample counter (IC3,4) is preset by an incoming line sync pulse inverted by IC2b, a position byte having been set up on DP0-7 by an 8-bit output port from the host computer.

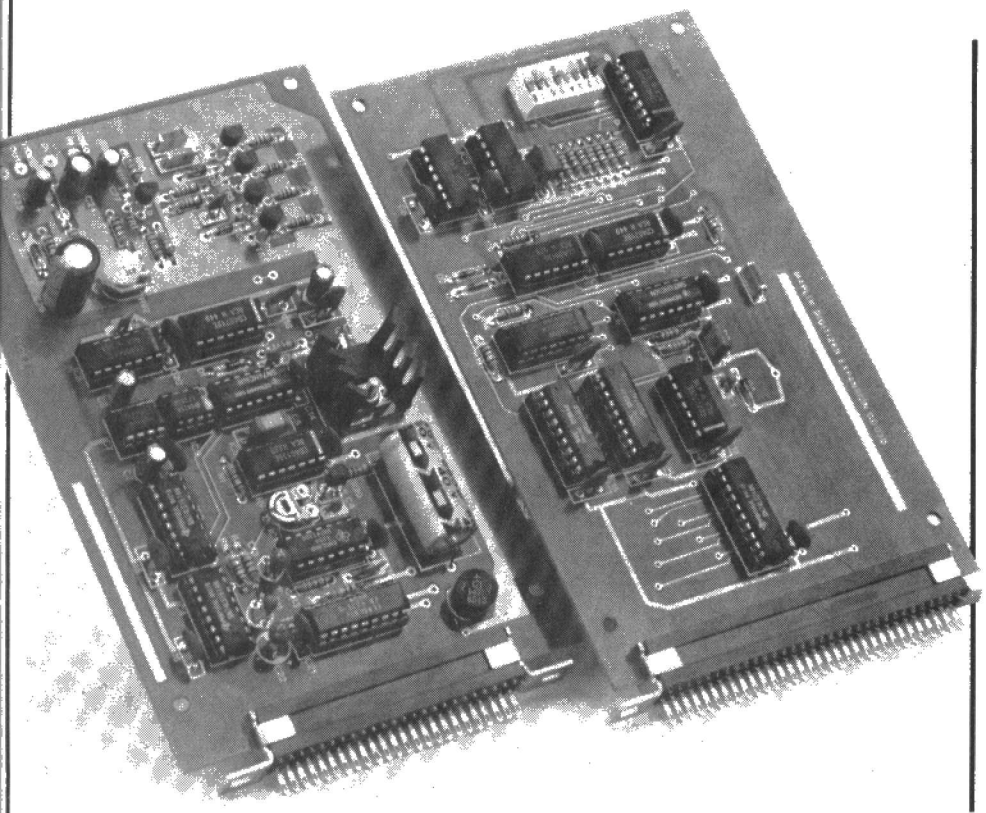
The line sync pulse also clocks flip-flop IC5 via OR gate IC6d, setting IC5 output high and enabling the oscillator IC1b via IC1c, which is used as a Schmitt Inverter.

This oscillator clocks the sample counter at a frequency determined by RV1/C4 (≃4MHz) and causes it to count down to zero and carry, disabling the oscillator by resetting IC5 via IC6d to prevent any further sample pulses during the present line.

The carry pulse is inverted by IC2c, and charges C9 which then discharges through R2, lengthening the pulse inverted by IC2a to operate the analogue switch IC8. This connects DC restored video from C25/D2 to the hold capacitor C8, which charges to the video voltage. The lengthened carry pulse is also inverted by IC2f whose output goes to the 'Start of Conversion' input on the analogue to digital converter IC10. When the pulse ends, the analogue switch opens and the 'Held' video voltage is applied to IC10 via IC9, a high input impedence op-amp connected as a voltage follower, i.e. unity gain.

The End Of Conversion (EOC) output from IC10 goes low enabling the clock oscillator IC1d via an emitter follower TR6 and IC1a which is connected as a Schmitt Inverter. After the ninth cycle of the oscillator, the EOC output of IC10 goes high, disabling IC1d and indicating end of conversion. This signal is sent to the host computer, indicating that the output of the A/D converter is valid. The host computer reads and stores the data on P(DA) via an 'X' bit input port, where 'X' is the required number of luminance bits.

IC7 is a voltage converter which produces a −5 Volt supply for IC9 and IC10.



Construction

Referring to the Parts List and PCB layout diagram (Figure 2), insert and solder veropins 1 to 6 from the underside of the board (Side 1) and fit Link 1 if termination of the video signal is required. Insert and solder in position all resistors, capacitors and diodes, taking note of polarity.

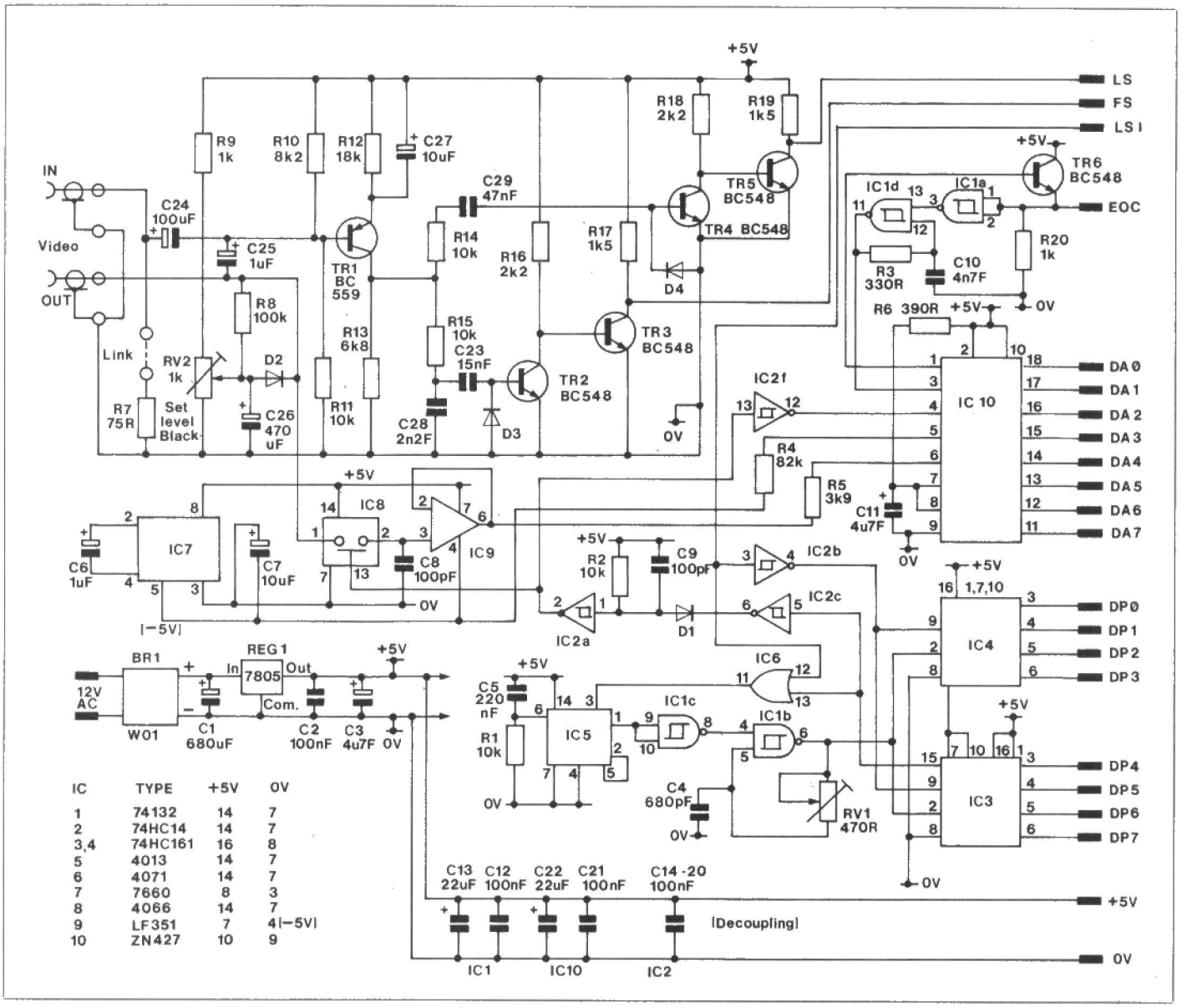
Insert and solder all IC sockets, transistors, BR1 and mount REG1 using the insulating washer and heatsink supplied, first smearing mating surfaces with heat transfer compound (not supplied).

Double check your work for short circuits, components in wrong places, etc. Five minutes careful examination of your work now may save much time and expense later.

Plug IC7 into its socket, ensuring correct orientation.

Testing

Minimum system I/O requirement is one 8-bit output port and one 8-bit input port. This allows for up to 5 bits of luminance information, which should be



IC	TYPE	+5V	0V
1	74132	14	7
2	74HC14	14	7
3,4	74HC161	16	8
5	4013	14	7
6	4071	14	7
7	7660	8	3
8	4066	14	7
9	LF351	7	4[−5V]
10	ZN427	10	9

Figure 1. Digitiser Circuit

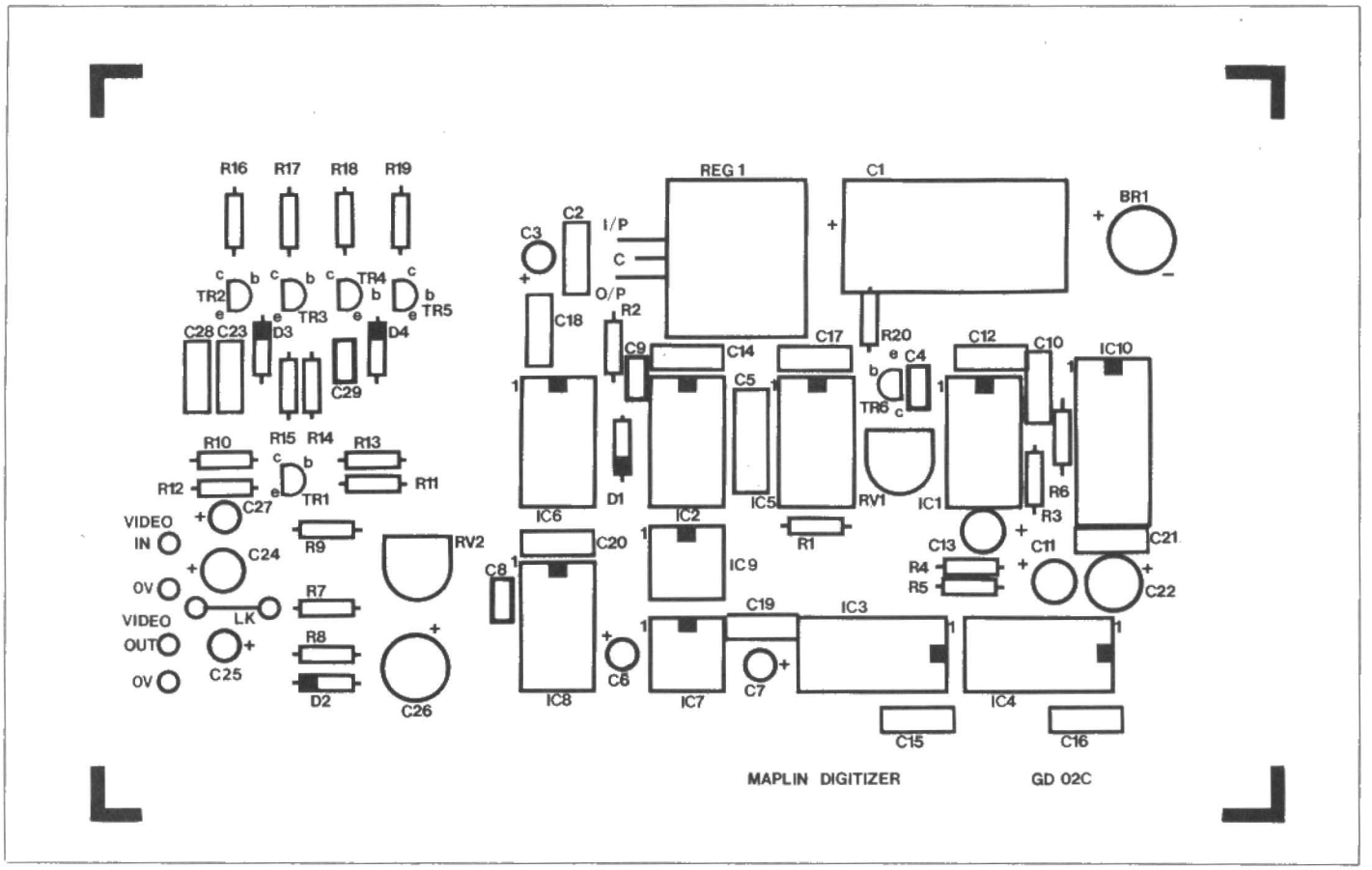


Figure 2. Digitiser PCB Layout

adequate for most microcomputer systems. For example wiring to host computer see Figure 3.

Without connecting the I/O lines to the host computer, apply power to the circuit and check for +5V and −5V supply rails. If either of these are not present, or read high, then switch off immediately and re-check your work.

If all is well however, switch off and insert the remaining IC's noting orientation. Connect a suitable source of video to the input of the Digitiser and the I/O lines to the host computer. Set the computer output port (PD in the example) to a valid position value, e.g. decimal 100. If an oscilloscope is available, check that TTL level Line Sync and Frame Sync pulses are present at LS and FS, respectively.

With LS connected to LSI and an Oscilloscope to IC3 pin 2, 4MHz clock pulses should be present, gated at line rate (64μs). Set RV1 to about half travel and RV2 fully anticlockwise. Connect the scope to IC10 pin 4, where short pulses at line frequency should be present. Lastly, connect the scope to IC10 pin 3; the scope should display bursts of pulses at approximately 600kHz, gated at line rate. If an Oscilloscope is not available, a Logic Probe will give a fair indication that pulses are present at the above points.

Line and Frame Sync pulses may also be detected by software, as indeed they must be during operation of the Digitiser.

Programming and Use

Making use of this single board system is only possible using machine code software, since real time detection of sync pulses is necessary to determine the vertical position of the sample point within the frame.

For those who are not keen on writing machine code, or wish to simplify the programming, a controller board has been designed to make use of the Digitiser as simple as possible, enabling a simple BASIC language program to operate the unit.

For those who are comfortable writing in machine language or assembly code, the program requirements are as follows:-

1. Set an 8-bit port for output (position port). Set an 8-bit port for input (luminance on low nibble and EOC, FS and LS on the three most significant bits. (LS should be the most significant bit for fast testing.) Reserve a block of memory for luminance information,

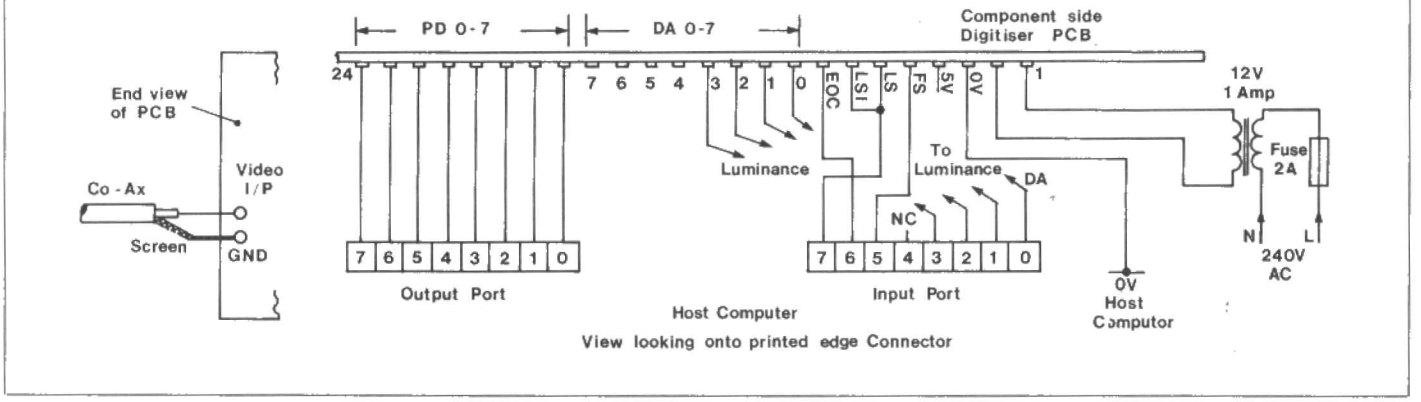
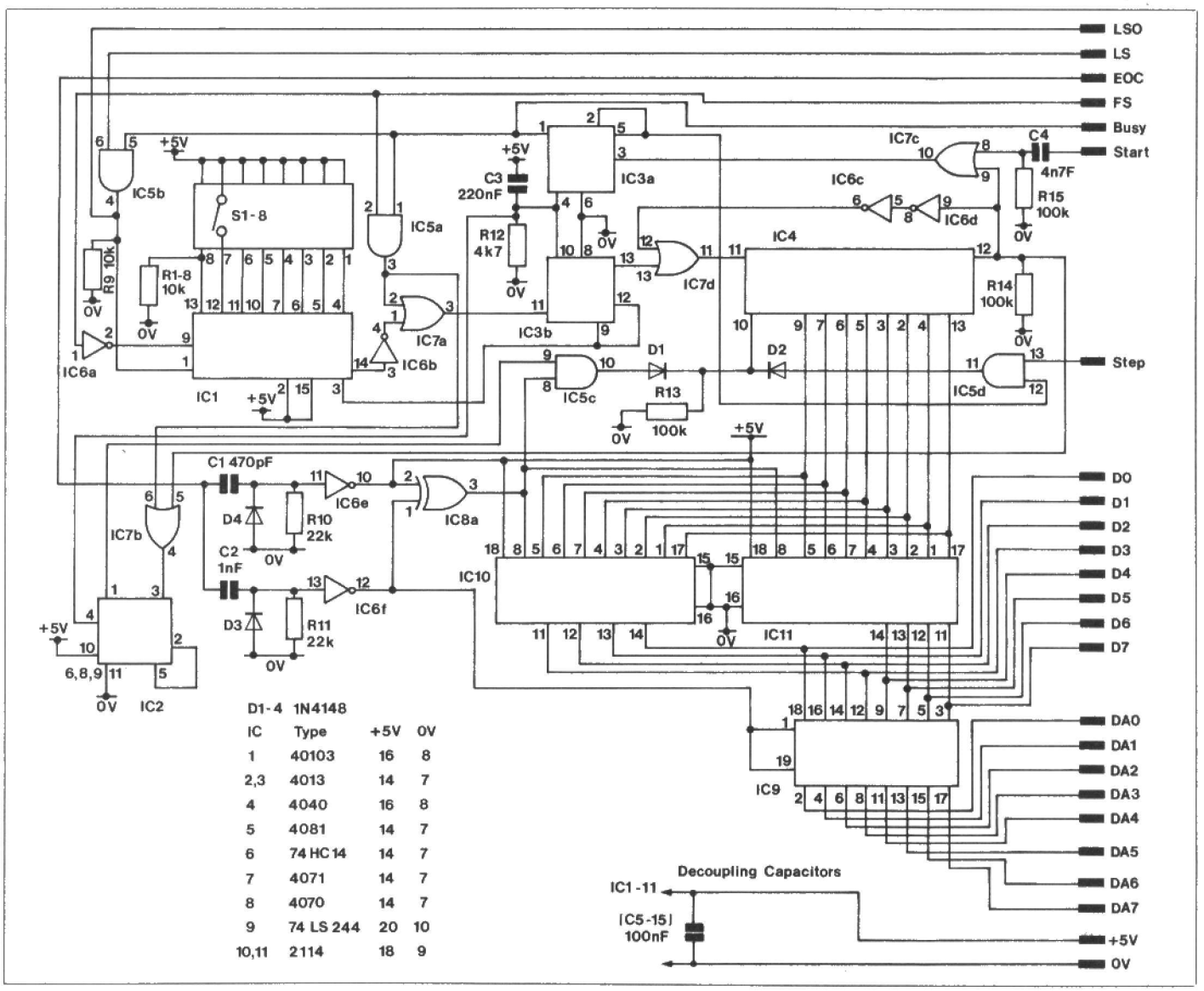


Figure 3. Board System Wiring



D1-4 1N4148

IC	Type	+5V	0V
1	40103	16	8
2,3	4013	14	7
4	4040	16	8
5	4081	14	7
6	74HC14	14	7
7	4071	14	7
8	4070	14	7
9	74LS244	20	10
10,11	2114	18	9

Figure 4. Controller Circuit

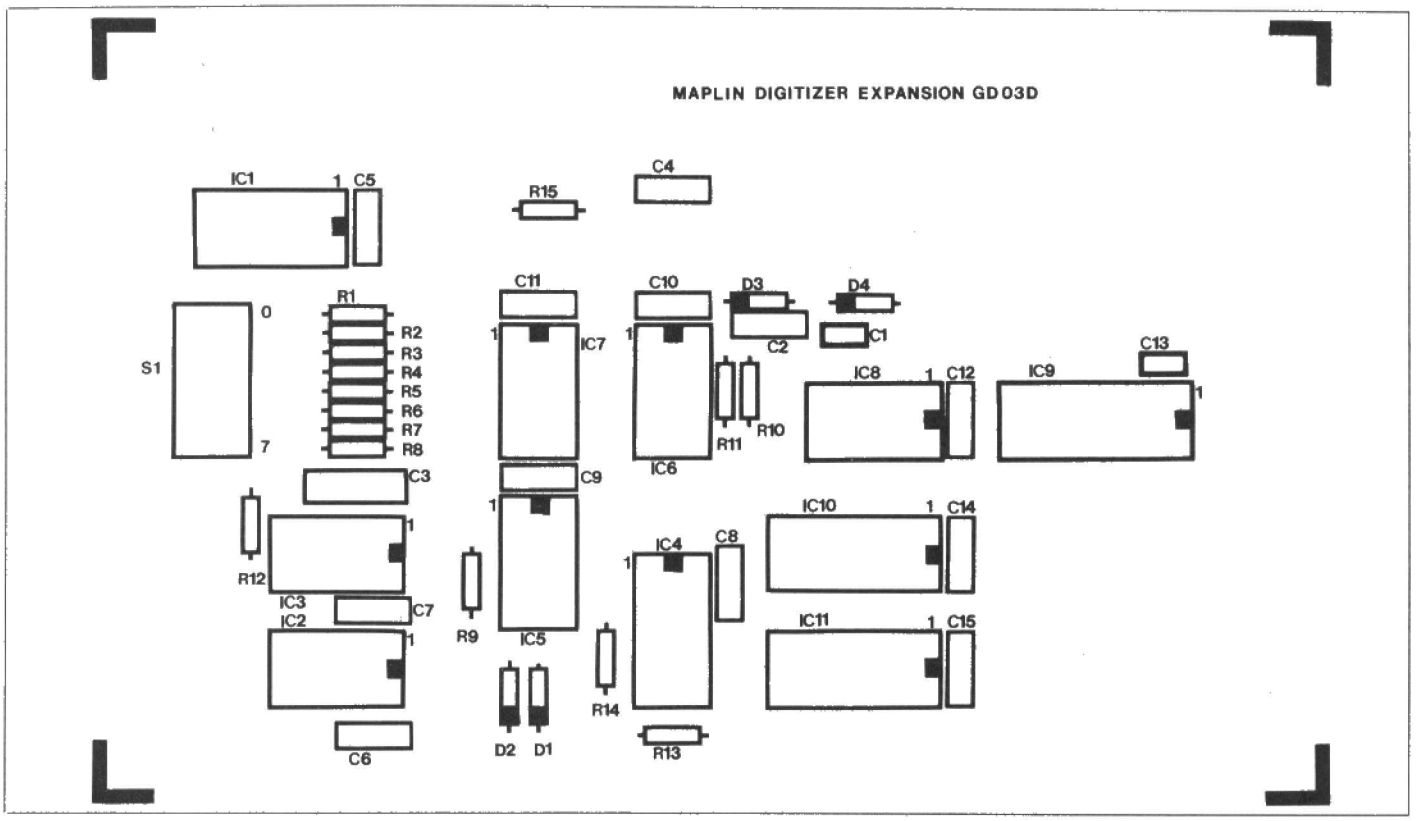


Figure 5. Controller PCB Layout

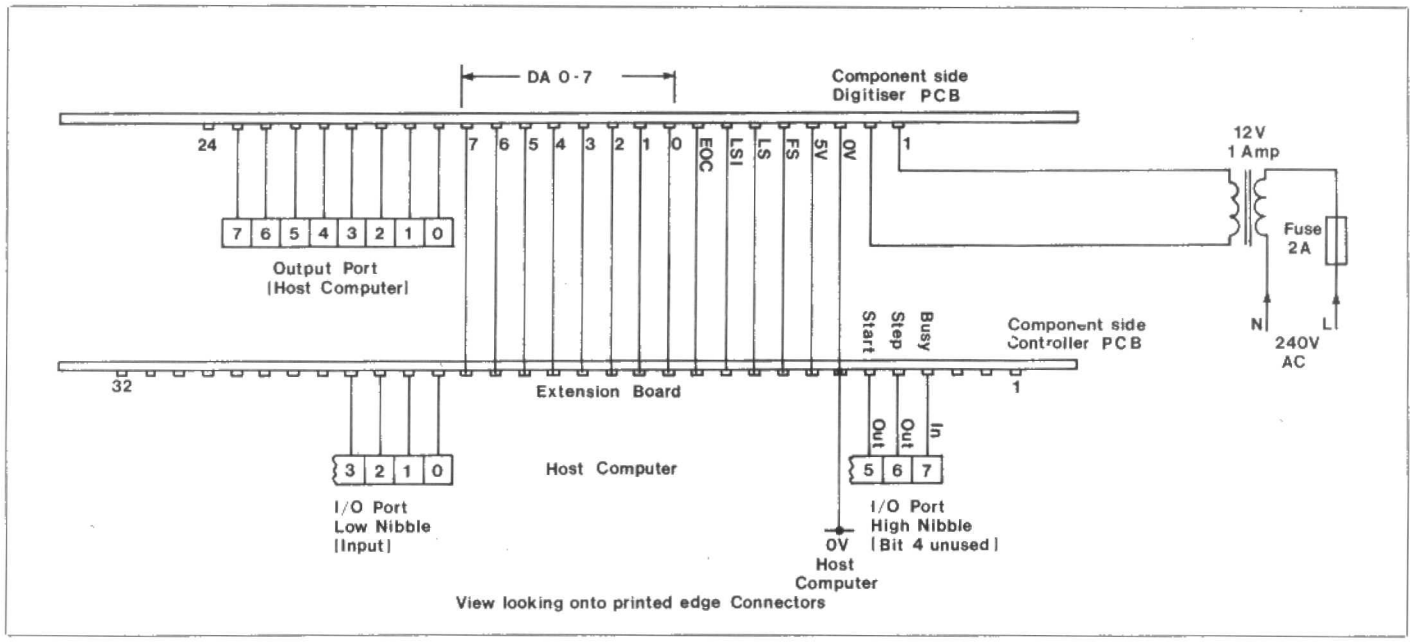


Figure 6. Two Board System Wiring

set up pointers to this block. Send initial position byte to position port (254 is extreme left, 0 is extreme right).

2. Wait for a Frame Sync pulse (test FS bit until high). Wait for end of Frame Sync (FS bit low).
3. By testing the LS bit in the same way, count the number of lines down the screen until the required line to start conversion occurs.
4. Reset the line counter to zero.
5. Wait for EOC bit to go low, then high.
6. Read luminance bits, store via pointer and increment pointer.
7. Compare current line scan number with maximum (312 or less, depending on requirement). If ⩾ max then go to step 9.
8. Increment line counter. Wait for Line Synch. as before. Go to step 5.
9. Column stored. Compare current position byte with final position number. If ⩾ max then go to step 11.
10. Increment position port. Go to step 2.
11. Frame stored. Process information to display on microcomputer.

In this way, the picture is built up in memory, column by column (one column for each frame, 20ms) in about 5 seconds (for a full width picture). Once a picture is being stored and displayed, contin-

VIDEO DIGITISER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,2,11,14,15	10k	5	(M10K)
R3	330R	1	(M330R)
R4	82k	1	(M82K)
R5	3k9	1	(M3K9)
R6	390R	1	(M390R)
R7	75R	1	(M75R)
R8	100k	1	(M100K)
R9,20	1k	2	(M1K)
R12	18k	1	(M18K)
R13	6k8	1	(M6K8)
R16,18	2k2	2	(M2K2)
R17,19	1k5	2	(M1K5)
R10	8k2	1	(M8K2)
RV1	470R Hor Sub-Min Preset	1	(WR54J)
RV2	1k Hor Sub-Min Preset	1	(WR55K)
CAPACITORS			
C1	680µF 40V Axial Electrolytic	1	(FB79L)
C2,12,14-21	100nF Minidisc	10	(YR75S)
C3	4µ7F 63V P.C. Electrolytic	1	(FF03D)
C4	680pF Ceramic	1	(WX66W)
C5	220nF Poly Layer	1	(WW45Y)
C6,25	1µF 100V P.C. Electrolytic	2	(FF01B)
C7,27	10µF 50V P.C. Electrolytic	2	(FF04E)
C8,9	100pF Ceramic	2	(WX56L)
C10	4n7F Poly Layer	1	(WW26D)
C11	4µ7F 16V Tantalum	1	(WW64U)
C13,22	22µF 16V Tantalum	2	(WW72P)
C23	15nF Poly Layer	1	(WW31J)
C24	100µF 10V P.C. Electrolytic	1	(FF10L)
C26	470µF 16V P.C. Electrolytic	1	(FF15R)
C28	2n2F Poly Layer	1	(WW24B)
C29	47nF Minidisc	1	(YR74R)

SEMICONDUCTORS			
D1-D4	1N4148	4	(QL80B)
TR1	BC559	1	(QQ18U)
TR2,3,4,5,6	BC548	5	(QB73Q)
BR1	W01	1	(QL38R)
REG1	µA7805UC	1	(QL31J)
IC1	74132	1	(WH03D)
IC2	74HC14	1	(UB10L)
IC3,4	74HC161	2	(UB41U)
IC5	4013BE	1	(QX07H)
IC6	4071BE	1	(QW43W)
IC7	7660	1	(YY75S)
IC8	4066BE	1	(QX23A)
IC9	LF351	1	(WQ30H)
IC10	ZN427	1	(UF40T)
MISCELLANEOUS			
	Digitiser PCB	1	(GD02C)
	Vaned Heatsink	1	(FL68N)
	Kit (P) Plas	1	(WR23A)
	DIL Socket 8-Pin	2	(BL17T)
	DIL Socket 14-Pin	5	(BL18U)
	DIL Socket 16-Pin	2	(BL19V)
	DIL Socket 18-Pin	1	(HQ76H)
	Connectector 124	1	(FL85G)
	Edge Conn. End Bkt.	2	(YR58N)
	Bolt 6BA x ½in.	1 Pkt	(BF06G)
	Nut 6BA	1 Pkt	(BF18U)
	Transformer 12V 1A	1	(WB25C)

A kit of parts is available for this project:
Order As LK95D (Digitiser Kit) Price £41.95
The following item included in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Digitiser PCB **Order As GD02C Price £11.95**

uously, adjustment of RV1 will vary the aspect ratio to suit the graphics mode of the host computer.

The digitised pictures could be stored on an 'album' disk or used as backgrounds, for games for example. Some animation may be possible, if the host computer allows screen paging, by flipping between several stored images with slightly different subject positions.

However the stored images are used, this Digitiser provides a novel and interesting use for the home computer when the games begin to pall, and an answer to that recurrent question: 'What can you do with a computer?'

Controller

This is an optional extension of the Video Digitiser, which greatly simplifies the programming required to use it. Using the Controller, software detection of Frame and Line Sync pulses is no longer necessary, this being handled solely by hardware. In operation, a start pulse is sent to the controller board and the busy line is monitored until it goes low. This indicates that a column of data has been stored which is read by the host computer, using the step input to scan through the stored information. A new position byte is sent to the Digitiser and the process repeated until the whole picture has been stored.

Circuit Description

In Figure 4, upon receipt of a start pulse at CLK of IC3a via OR gate IC7c and C4/R15, a pulse length limiting network, the Q output of IC3a goes high, gating Line Sync pulses to LSO (Line Sync Out) which is connected to the sample pulse generating circuit on the Digitiser board. IC3a Q output also gates Frame Sync to IC3b via OR gate IC7a, causing IC3b Q output to go high upon receipt of the next Frame Sync pulse (start of picture). This holds line counter (IC4) reset via OR gate IC7d, while the $\overline{Q}$ output of IC3b enables counter IC1, a presettable counter that counts a number of 'wasted' lines before carrying, i.e. sets vertical start position of digitised picture. Note, this number should not be set (Dipswitch) higher than 55.

The carry pulse from IC1 is inverted and clocks IC3b, reseting it, via IC7a. IC1 is disabled by $\overline{Q}$ output of IC3b going high and IC4 enabled by Q going low. IC2 was clocked by Frame Sync via IC7,5 and its Q output gates $\overline{\text{CHIP SELECT}}$ pulses from IC8 through to clock input of IC4. These $\overline{\text{CHIP SELECT}}$ pulses are derived from the end of conversion output of the Digitiser board, as are $\overline{\text{WRITE ENABLE}}$ and $\overline{\text{ENABLE}}$ for the RAM and RAM Buffer, respectively.

$\overline{\text{WRITE ENABLE}}$ comes from pulse shaping circuit C1/R10 via IC6 and the longer ENABLE pulse from C2/R11 via IC6. $\overline{CS}$ and $\overline{E}$ are exclusively OR'ed by IC8 to produce $\overline{CS}$. Using this method to produce $\overline{CS}$ ensures that no conflict is possible on the Data Bus D0–D7 between the RAM and the Buffer (IC10/11 and IC9), since $\overline{CS}$ can only be low (active) when either:-

a) $\overline{WE}$ and $\overline{E}$ are both low. (Buffer has control of Bus) or,

b) $\overline{WE}$ and $\overline{E}$ are both high. (RAM has control of Bus).

Under the control of these signals, the data from the Digitiser is passed via buffer IC9 to RAM (IC10/11 for eight bit resolution) and the line counter (IC4) advanced to the next line address. This process continues for each line until IC4 carries, resetting itself via IC6/7 and resetting IC3a via IC7c. Line and Frame Sync pulses are no longer gated to the counters/flip-flops and the busy line goes low, indicating that a vertical column of screen data has been stored in the controller RAM, and is ready to be transferred to the host computer.

The 'step' input is now enabled by the $\overline{Q}$ output of IC3a and data may be transferred by reading the Data Bus and applying a step pulse, which clocks IC4, stepping it to the next line address, until all data has been read (≤256 lines depending on system requirement).

Listing 1.

```
5 GRAPHICS 9
10 REM .*   SET UP PORTS      *
20 POKE 54019,56
30 POKE 54017,255
40 POKE 54019,60
50 POKE 54018,56
60 POKE 54016,112
70 POKE 54018,60
80 C=0
100 PA=54016:PB=54017
200 POKE PB,230
250 POKE PA,64:POKE PA,0
300 IF PEEK(PA)/128>=1 THEN GOTO 300
400 FOR X=0 TO 191:LUM=PEEK(PA)
410 GOSUB 2000:POKE PA,32
420 POKE PA,0:NEXT X
430 C=C+1:POKE PB,230-C
500 GOTO 250
2000 IF C=80 THEN GOTO 2000
2010 COLOR LUM:PLOT C,X:RETURN
```

DIGITISER CONTROLLER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1-9	10k	9	(M10K)
R10,11	22k	2	(M22K)
R12	4k7	1	(M4K7)
R13,14,15	100k	3	(M100K)
CAPACITORS			
C1	470pF Ceramic	1	(WX84U)
C2	1nF Poly Layer	1	(WW22Y)
C3	220nF Poly Layer	1	(WW45Y)
C4	4n7F Poly Layer	1	(WW26D)
C5-15	100nF Minidisc	11	(YR75S)
SEMICONDUCTORS			
D1-4	1N4148	4	(QL80B)
IC1	40103BE	1	(QW61R)
IC2,3	4013BE	2	(QX07H)
IC4	4040BE	1	(QW27E)
IC5	4081BE	1	(QW48C)
IC6	74HC14	1	(UB10L)
IC7	4071BE	1	(QW43W)
IC8	4070BE	1	(QX26D)
IC9	74LS244	1	(QQ56L)
IC10,11	2114	2	(QW12N)
MISCELLANEOUS			
	Digitiser Controller PCB	1	(GD03D)
S1	DIL Switch SPST (Octal)	1	(XX27E)
	Connector 132	1	(FL86T)
	Edge Conn. End Bkt.	2	(YR58N)
	DIL Socket 18-Pin	2	(HQ76H)
	DIL Socket 20-Pin	1	(HQ77J)
	DIL Socket 14-Pin	6	(BL18U)
	DIL Socket 16-Pin	3	(BL19V)

A kit of parts is available for this project:
Order As LK96E (Digitiser Controller Kit) Price £29.95
The following item included in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Digitiser Controller PCB **Order As GD03D Price £11.95**

Construction

Locate and solder all resistors, capacitors and diodes, noting polarities. Fit and solder Dipswitch and all IC sockets, locating Dipswitch with the writing on its side facing the edge of the board, and the polarity notches of the IC sockets matching the square block marked on each IC legend. See Figure 5. Carefully insert all IC's in their respective positions, taking note of correct orientation. Wire the edge connector as shown in Figure 6, referring to your computer manual or instructions for your I/O port, where applicable. Keep all wiring between the boards and the computer as short as possible to avoid corruption of data. Take care to check all joints/connections for short circuits, dry joints, etc.

Testing

Plug both boards into their edge connectors and apply power. Check the

5V supply using a multimeter. IC3 pins 1 and 13, IC2 pin 1 should all be low (<1V), relative to 0V. All being well, switch off and connect the circuits to the host computer and video source as shown in Figure 6.

Programming

Listing 1 shows a BASIC language program to operate the Digitiser. The addresses given relate to the port addresses of the Atari 400/800 computers. A BASIC program will take several minutes to complete the screen display, but has the advantage of being very quick and easy to write. For those who desire faster operation, a machine code program will be required. An example (Listing 2) is provided in 6502 assembly language, again for the Atari 400/800 computers, although no explanation of this program will be included here, this being beyond the scope of the present article.

Throughout this article, it has been assumed that the reader has a basic understanding of the construction of a video signal. For those who wish to gain some knowledge on the subject, the following book is recommended:

Questions and Answers on Video by Steve Money, available from Maplin (Stock Code WG77J).

Listing 2.

```
10    *=$7000
20  PORTA=$D300
30  PORTB=$D301
40  PACTL=$D302
50  PBCTL=$D303
60  NMIEN=$D40E
70  IRQEN=$D20E
80  POKMSK=$0010
90  DMACTL=$D400
0100  SDMCTL=$022F
0110  SAVMC=$0058
0120  MASK=$06F9
0130  LINES=$06FA
0140  POSIT=$06FB
0150  SCNCOL=$06FC
0160  OFFSET=$00D4
0170  FINCOL=$06FE
0180            PLA
0190  INIT      LDA #$00
0200            STA LINES
0210            LDA #240
0220            STA POSIT
0230            LDA SAVMC
0240            STA SCNCOL
0250            LDA SAVMC+1
0260            STA SCNCOL+1
0270            CLC
0280            CLD
0290            TAX
0300            LDA SCNCOL
0310            ADC #40
0320            STA FINCOL
0330            BCC NOINT
0340            INX
0350  NOINT     STX FINCOL+1
0360            LDA#$38
0370            STA PBCTL
0380            STA PACTL
0390            LDA#96
0400            STA PORTA
0410            LDA#$FF
0420            STA PORTB
0430            LDA#$3C
0440            STA PBCTL
0450            STA PACTL
0460  START     LDA SCNCOL
0470            STA OFFSET
0480            LDA SCNCOL+1
0490            STA OFFSET+1
0500            LDA POSIT
0510            STA PORTB
0520  TOG       LDA#64
0530            STA PORTA
0540            JSR DELAY
0580            LDA#0
0590            STA PORTA
0600  HI        BIT PORTA
0610            BMI HI
0620  GETLUM    LDX PORTA
0630            LDA POSIT
0640            LSR A
0645            LSR A
0650            BCC MULT
0660            TXA
0662            LDX#240
0664            STX MASK
0670            AND #$0F
0680            JMP STORE
0690  MULT      TXA
0692            LDX#15
0694            STX MASK
0700            ASL A
0710            ASL A
0720            ASL A
0730            ASL A
0740  STORE     LDY#$00
0750            ORA (OFFSET),Y
0760            STA (OFFSET),Y
0762            LDY#40
0764            LDA(OFFSET),Y
0765            AND MASK
0766            STA(OFFSET),Y
0770  NEWROW    CLC
0780            CLD
0790            LDA OFFSET
0800            ADC #40
0810            STA OFFSET
0820            BCC LNCHK
0830            CLC
0840            INC OFFSET+1
0850  LNCHK     INC LINES
0860            LDA LINES
0870            CMP #191
0880            BCC STEP
0890            LDA #$00
0900            STA LINES
0910  ODD       LDA POSIT
0920            LSR A
0925            LSR A
0930            BCC PICFIN
0940            CLC
0950            LDA SCNCOL
0960            ADC #$01
0970            STA SCNCOL
0980            BCC PICFIN
0990            INC SCNCOL+1
1000  PICFIN    DEC POSIT
1005            DEC POSIT
1010            LDA SCNCOL
1020            CMP FINCOL
1030            BCC NEWCOL
1040            LDA SCNCOL+1
1050            CMP FINCOL+1
1060            BCC NEWCOL
1070  FIN       RTS
1080  STEP      LDA#32
1090            STA PORTA
1100            JSR DELAY
1150            LDA#0
1160            STA PORTA
1170            JMP GETLUM
1180  NEWPIC    LDA#$16
1190            STA POSIT
1200            LDA SAVMC+1
1210            STA SCNCOL+1
1220            LDA SAVMC
1230            CLC
1240            ADC #40
1250            STA SCNCOL
1260            BCC NEWCOL
1270            INC SCNCOL+1
1280  NEWCOL    JMP START
1290  DIS       LDA #$00
1300            STA IRQEN
1310            STA POKMSK
1320            STA NMIEN
1330            STA DMACTL
1340            STA SDMCTL
1350            RTS
1360  ENA       LDA #$C0
1370            STA IRQEN
1380            STA POKMSK
1390            STA NMIEN
1400            LDA #34
1410            STA DMACTL
1420            STA SDMCTL
1430            RTS
1440  DELAY     LDX#30
1450  DOWN      DEX
1460            BNE DOWN
1470            RTS
```

MIXING IT

by Dave Goodman

Part 1 Using Maplin High Quality Mixer Modules

The Maplin range of HQ Mixer pre-amplifier modules serve as useful building blocks in audio circuits requiring high quality signal processing. General information and technical specifications are detailed here for various circuits and modules available – by popular demand! This first part describes some of the modules available, and in Part 2 more will be discussed and interconnecting between modules explained.

General Purpose Input Module

MODULE SPECIFICATIONS

Input Impedance	100kΩ (>60kΩ with pot)
Max Input Signal	275mV r.m.s. (777mV Pk)
Max Output Signal (Pre-Clipping)	2.2V r.m.s. (6.2V Pk)
I/P Signal for 450mV O/P	55mV r.m.s. (155mV Pk)
Frequency Response	20Hz – 200kHz (−3dB)
Distortion	0.025%
Noise	75μV (−80dB)

PSU +30V DC @ 25mA – both versions.

This circuit is for use with either pre-amplified signals or musical instruments such as keyboards, guitars etc. The overall circuit gain is approximately 9 times which makes this module unsuitable for very low output microphones, where the PU/MIC input module should be used. (This will be described in the next issue.) Input signal levels above 275mV can be handled by the infinitely variable sensitivity potentiometer which attenuates down to almost 0V. Output signal levels will start to clip above 6.2V Pk and the sensitivity control should be adjusted to prevent this, if distortion is not desired! Two versions of this module are available for stereo or

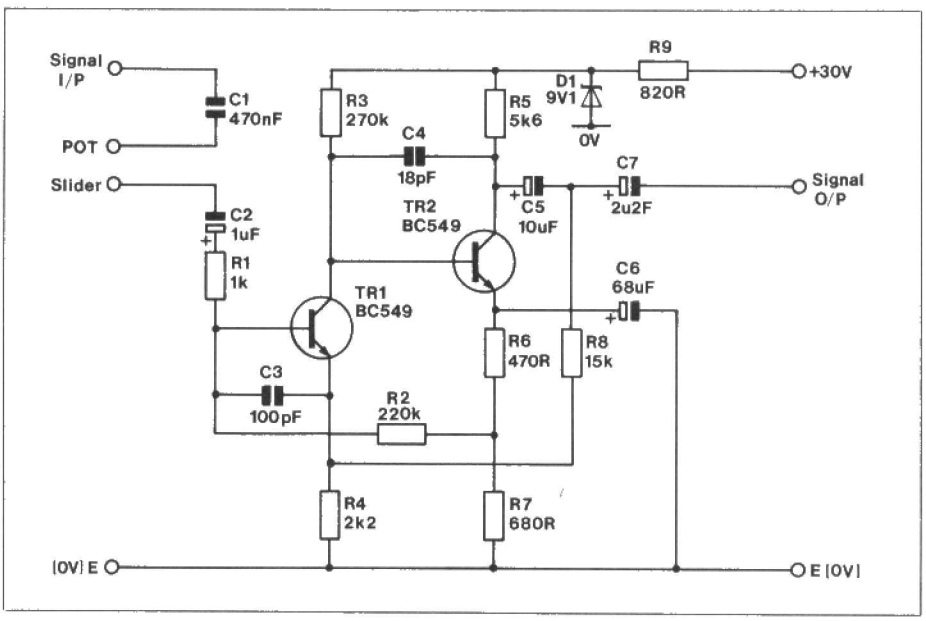


Figure 1. General Purpose Input Circuit

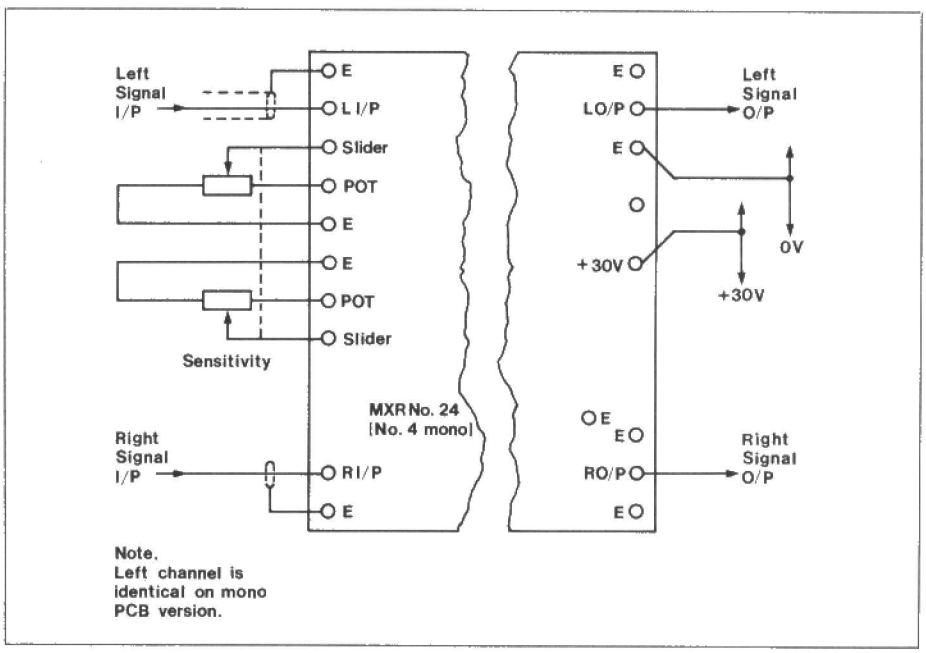


Figure 2. PCB Wiring

mono applications. Figure 1 shows the left (mono) channel only. The right (stereo) channel is identical except the components are designated with the prefix 10, i.e. R1 becomes R101, etc. Figure 2 shows wiring to the stereo PCB and Figure 3 illustrates how to wire the module to the sensitivity potentiometer.

Tone Control Module

MODULE SPECIFICATIONS

Bass Control	±18dB @ 20Hz
Treble Control	±16dB @ 10kHz
Frequency Response (Flat)	10Hz to 40kHz
Input Signal Level	Output Signal Level 450mV
Controls set 'Flat'	500mV r.m.s. 450mV
(Pre-Clipping)	4V r.m.s.
Distortion (@ 1kHz)	0.05%
Noise Level	150μV (−74dB)
PSU 30V DC @ 2.0mA (S), 1mA (M)	

Two versions of the tone control module are available in either mono (Figure 4 shows left channel only) and stereo and either of the two input-type modules may be used with this circuit. Figures 5/6 show the supply, input-output and control wiring arrangements. All signal carrying wires should be screened if cable lengths over 50mm are to be used, otherwise hum and noise will be a problem. A maximum input signal level of 450mV (1.27V Pk) is recommended as this allows full boost to be applied without distorting the waveform. Boosted output levels reach 11.5V Pk before clipping occurs. The module output is AC coupled to following stages and if balance or volume controls are not

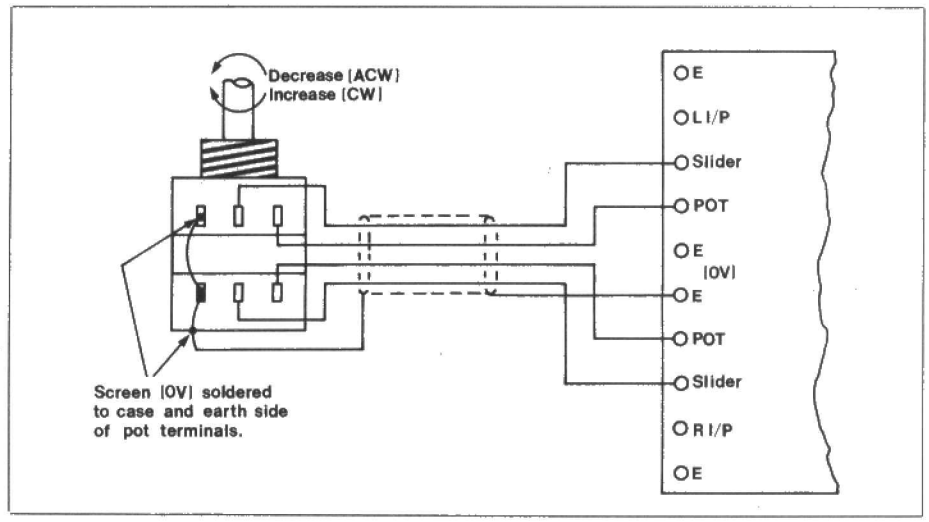


Figure 3. Wiring to Sensitivity Pot

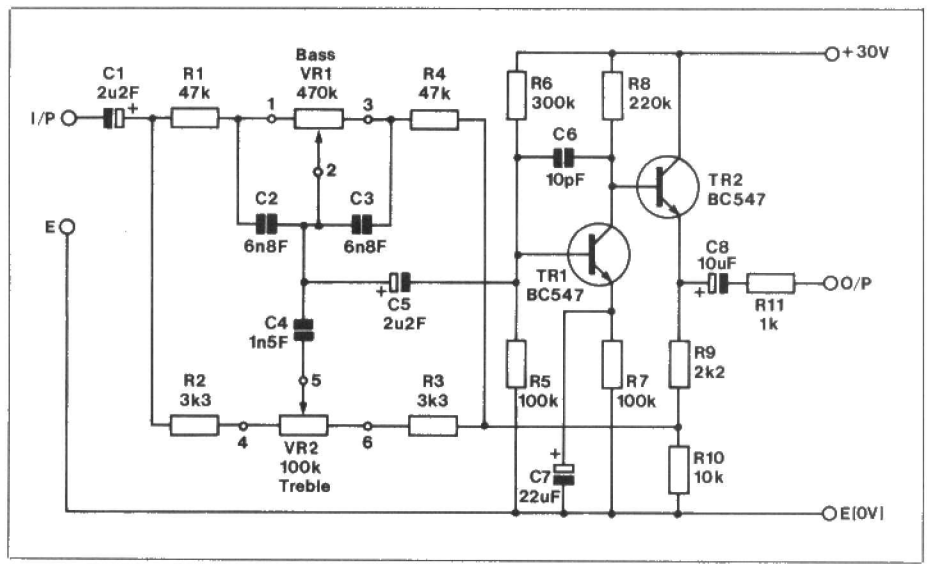


Figure 4. Tone Control Circuit (Mono)

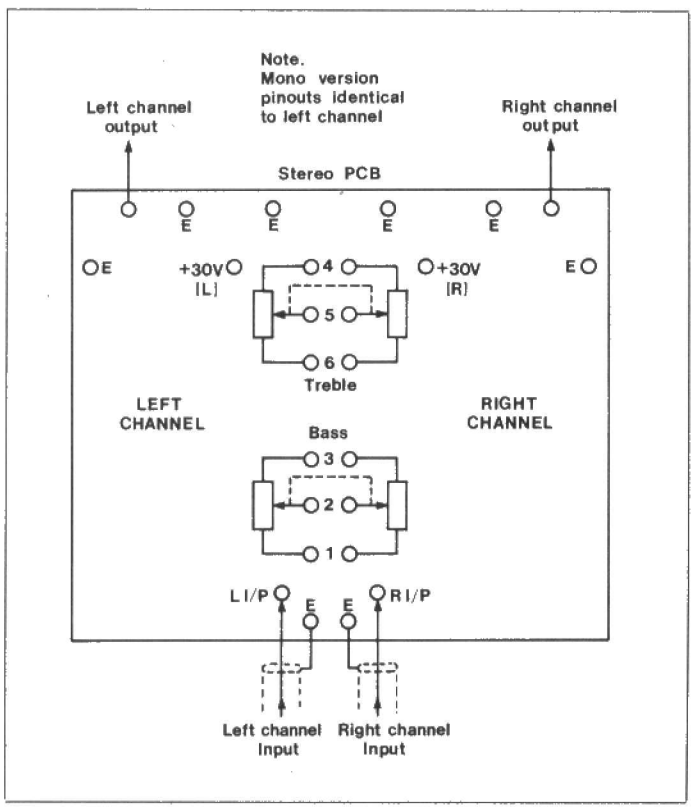


Figure 5. I/O Wiring

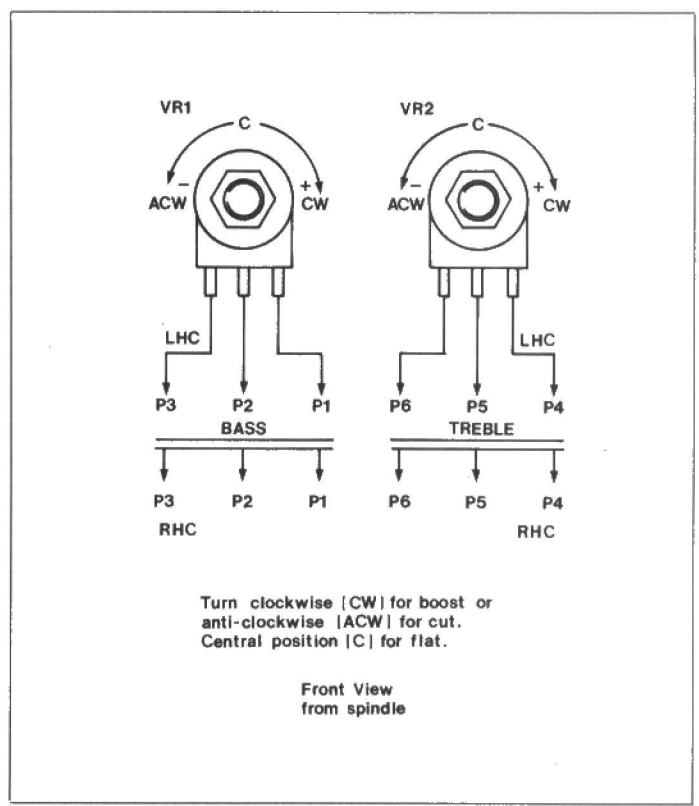


Figure 7. Boost and Cut

fitted here, then a 'pull down' resistor (4k7 – 10k) should be connected between output and GND (0V), otherwise the charged output coupling capacitor will develop a substantial DC voltage offset into the following stage. Figure 7 indicates Boost (+) and Cut (–) directions when potentiometers are wired as shown. Dual potentiometers are used on stereo modules and single potentiometers used on the mono version.

Peak Overload Detector Module

MODULE SPECIFICATIONS

Input Signal Range 1Hz – 10kHz (@ 450mV)
Min. Input Level 6mV r.m.s.
Adjustable to 450mV r.m.s. @ 1kHz
PSU 30V DC @ 12mA (Inc. LED)

The peak detector is a simple comparator circuit with a variable triggering threshold. Within the usable range of RV1, the trigger threshold can be set so that LED1 operates for input signals between 0.28 to 1.27V Pk. Higher levels will operate the LED even with RV1 set to minimum, although this condition could be accommodated by replacing R1 (or R2) for a bigger value. The module has two mixer inputs for mono or stereo use (either input pin can be used) and serves as a signal overload indicator to prevent clipping of signal waveforms and resulting distortion. RV1 would normally be set so that when distortion of output signals are noticeable, or measured, the LED is fully on. Figure 8 shows the circuit of the Peak Overload Detector and Figure 9 shows wiring to the module.

Filter Module

MODULE SPECIFICATIONS

Input Signal Level 5mV r.m.s. (14mV Pk) (Min. I/P Attenuation)
Max Output Signal 7V r.m.s. (20V Pk) (Pre-Clipping)
Filter Input Level Fully Variable By VR2 (VR102)
Frequency Response 25Hz – 40kHz Flat

Distortion	0.05%
Noise	45μV (–84dB)
Filter Range	5kHz, 7kHz, 10kHz, 15kHz and Flat
Roll-off	Variable –6dB to –18dB on Filter Range (Except Flat)

PSU +30V DC @ 5mA

The filter module shown in Figure 10 is a low pass filter with five switchable ranges having variable slope characteristics of –6 to –18dB per octave. Each filter range defines the cut off frequency where all signals above the selected value will be attenuated. The rate of attenuation can be varied for steep or shallow fall off curves as shown in Figure 11. The main use for this module is for equalisation of processed signals, that are to be fed to an output or power amp stage, or tape recording system. Distortion is kept low by utilising a purpose made pot-core (LR07H), available for the module, and circuit gain is high – in the order of x1400. Each output should be terminated with a 10k load, e.g. level control or fixed resistor to ground (0V) to maintain correct filtering action and circuit reactance, else quite high signal peaks will be produced at filter cut-off points.

The module comprises two PCB's; one holds amplifier stages and the other holds filtering components. The boards can be mounted side by side, or one above the other and holes have been drilled to facilitate this latter arrangement. Both modules are required for stereo or mono use!

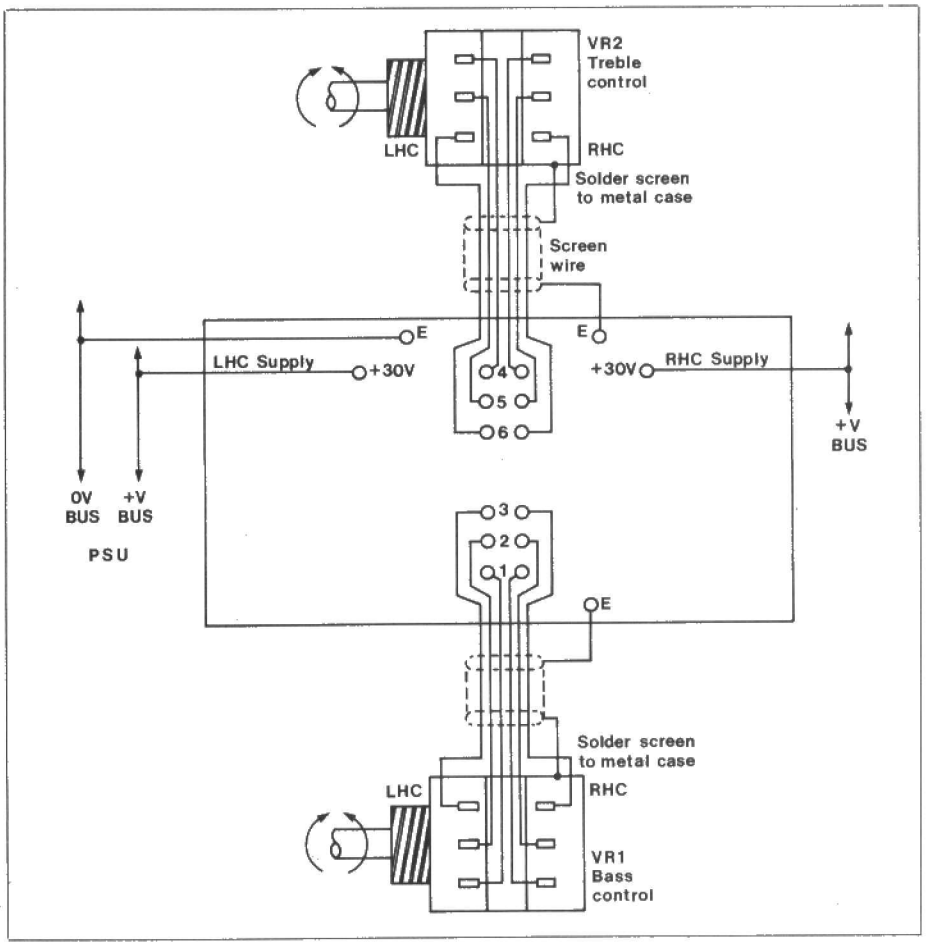


Figure 6. Wiring the Bass and Treble Pots

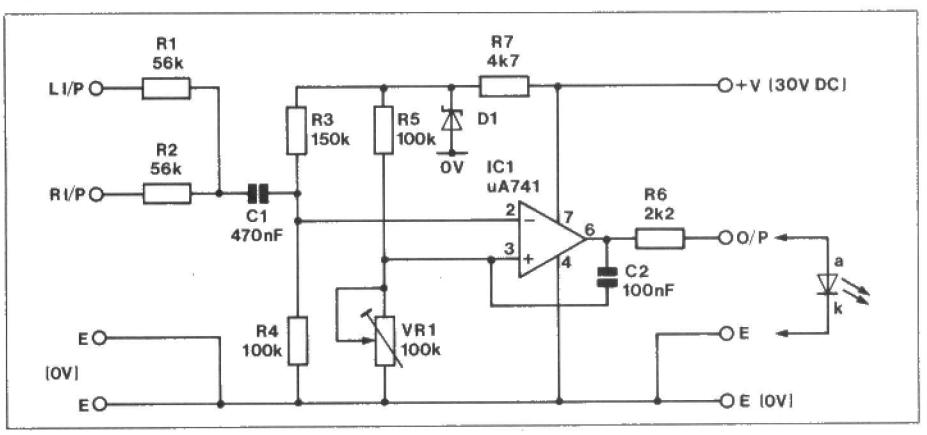


Figure 8. Peak Overload Detector Circuit

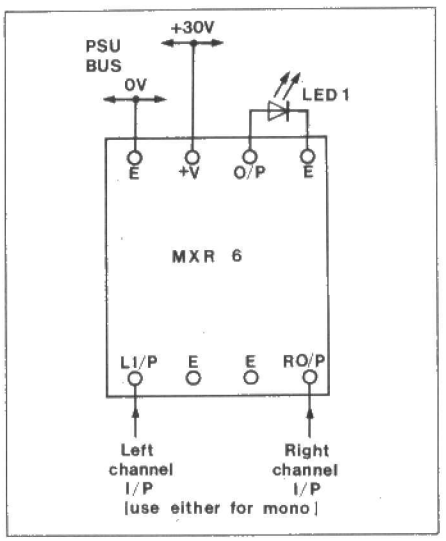


Figure 9. Wiring

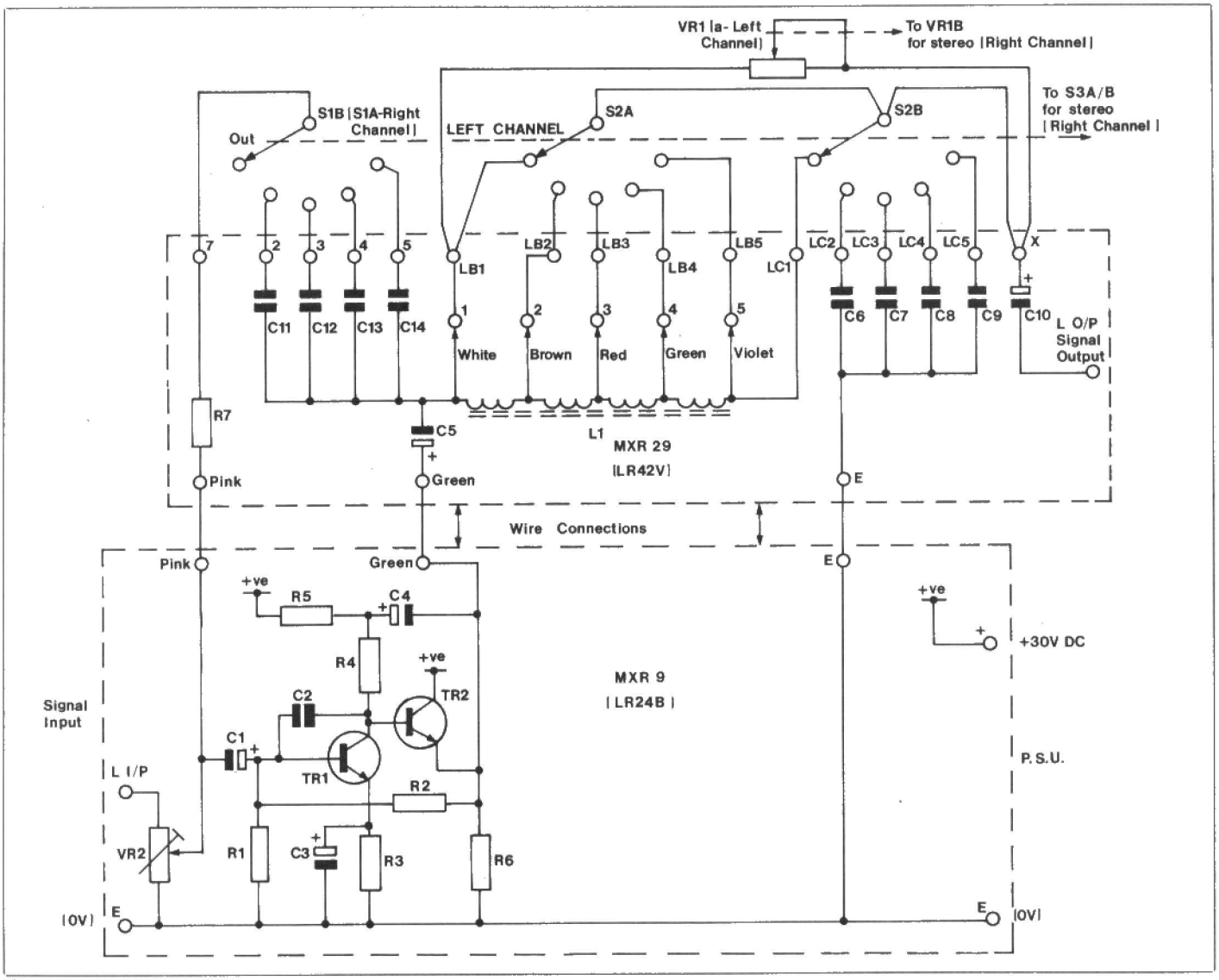


Figure 10. Filter Circuits (Left Channel)

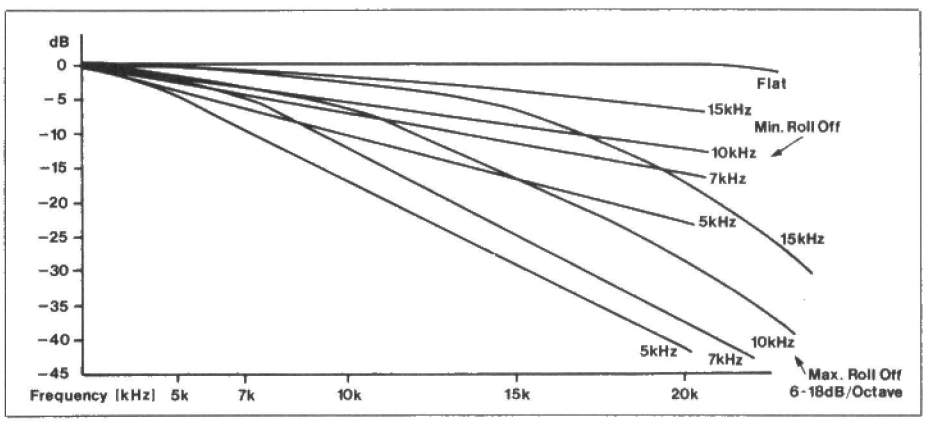


Figure 11. Filter Characteristics

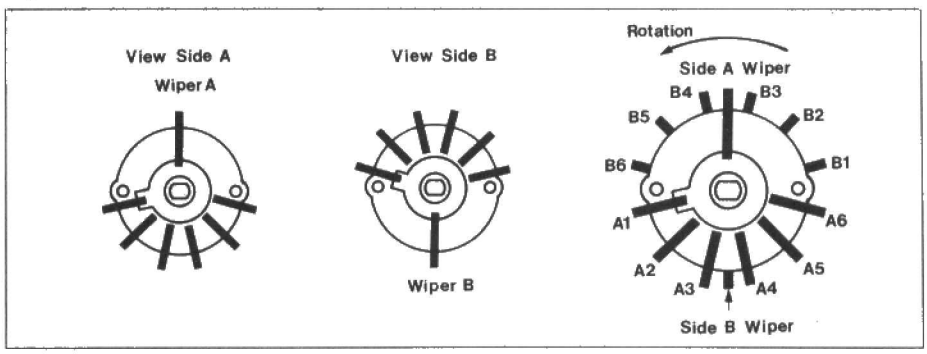


Figure 12. 2-Pole 6-Way Wafer

Three switching stages are needed for each channel and double sided wafer switches are recommended as shown in Figure 12. The make-shaft can be set to 5-way operation by re-inserting the locating peg as Figure 13 and each wafer slides over the shaft with their Side B offered first and facing the switch body housing (Figure 14). Figure 15 details wiring connections to and from and between both modules. Wiring from MXR 29 to wafer switches should be screened (multicore) and also screen VR1 wiring. MXR 29 0V(E) tracks are not commoned between left and right channels and separate 0V connections are required for this. Mixer Coil wire connections are colour-coded and should be fitted into their respective PCB positions as shown. The presets VR2 and VR102 are set to a position which maintains a suitable signal level throughout the module system, but it is not advisable to keep the wipers at the maximum – anticlockwise – position as the circuit is liable to oscillate due to the high gain characteristics of the input

GENERAL PURPOSE INPUT MODULE PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,101	1k	2	(M1K)
R2,102	220k	2	(M220K)
R3,103	270k	2	(M270K)
R4,104	2k2	2	(M2K2)
R5,105	5k6	2	(M5K6)
R6,106	470R	2	(M470R)
R7,107	680R	2	(M680R)
R8,108	15k	2	(M15K)
R9	820R	1	(M820R)
CAPACITORS			
C1,101	470nF Polyester	2	(BX80B)
C2,102	1μF Axial Electrolytic 100V	2	(FB12N)
C3,103	100pF Polystyrene	2	(BX28F)
C4,104	18pF Ceramic	2	(WX47B)
C5,105	10μF Axial Electrolytic 25V	2	(FB22Y)
C6,106	68μF Axial Electrolytic 16V	2	(FB44X)
C7,107	2μ2F Axial Electrolytic 100V	2	(FB15R)
SEMICONDUCTORS			
TR1,2,101,102	BC549	4	(QQ15R)
D1	BZY88C9V1 Zener	1	(QH13P)
MISCELLANEOUS			
	HQ Mixer No.24 (Stereo) PCB	1	(LR34M)
	HQ Mixer No.4 (Mono) PCB	1	(LR15R)
	Veropin 2145	1 Pkt	(FL24B)
OPTIONAL			
VR1	100k Pot Log (Mono)	1	(FW25C)
VR101	100k Dual Pot Log (Stereo)	1	(FX12N)

Kits and ready-built modules (excluding optional items) are available:
Order As LK81C (Gen. Purpose Input Kit (mono)) Price £2.95
Order As LK82D (Gen. Purpose Input Kit (stereo)) Price £4.50
Order As YM15R (Gen. Purpose Input Module (mono)) Price £3.95
Order As YM16S (Gen. Purpose Input Module (stereo)) Price £6.40

PEAK OVERLOAD DETECTOR MODULE PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,2	56k	2	(M56K)
R3	150k	1	(M150K)
R4,5	100k	2	(M100K)
R6	2k2	1	(M2K2)
R7	4k7	1	(M4K7)
VR1	Vertical Sub-min Preset 100k	1	(WR74R)
CAPACITORS			
C1	470nF Polyester	1	(BX80B)
C2	100nF Polyester	1	(BX76H)
SEMICONDUCTORS			
IC1	μA741 Op-Amp 8 pin	1	(QL22Y)
D1	BZY88C6V2	1	(QH09K)
MISCELLANEOUS			
	HQ Mixer No.6 PCB	1	(LR21X)
	Veropin 2145	1 Pkt	(FL24B)
SKT 1	IC Socket DIL 8 pin	1	(BL17T)
OPTIONAL			
LED 1	Red LED	1	(WL27E)

A kit and ready-built module (excluding optional item) is available:
Order As LK85G (Peak Overload Detector Kit) Price £2.20
Order As YM19V (Peak Overload Detector Module) Price £3.20

TONE CONTROL MODULE PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,R4,101,104	47k	4	(M47K)
R2,3,102,103	3k3	4	(M3K3)
R5,7,105,107	100k	4	(M100K)
R6,106	300k	2	(M300K)
R8,108	220k	2	(M220K)
R9,109	2k2	2	(M2K2)
R10,1010	10k	2	(M10K)
R11,1011	1k	2	(M1K)
CAPACITORS			
C1,5,101,105	2μ2F Axial Electrolytic 100V	4	(FB15R)
C2,3,102,103	6n8F Polystyrene	4	(BX66W)
C4,104	1n5F Polystyrene	2	(BX58N)
C6,106	10pF HV Disc	2	(BX05F)
C7,107	22μF Axial Electrolytic 100V	2	(FB31J)
C8,108	10μF Axial Electrolytic 63V	2	(FB23A)
SEMICONDUCTORS			
TR1,2,101,102	BC547	4	(QQ14Q)
MISCELLANEOUS			
	HQ Mixer No.5 (Mono) PCB	1	(LR16S)
	HQ Mixer No.25 (Stereo) PCB	1	(LR35Q)
	Veropins 2145	1 Pkt	(FL24B)
OPTIONAL			
VR1	470k Pot Lin. (Mono)	1	(FW07H)
VR2	100k Pot Lin. (Mono)	1	(FW05F)
VR101	470k Pot Dual Lin. (Stereo)	1	(FW90X)
VR102	100k Pot Dual Lin. (Stereo)	1	(FW88V)

Kits and ready-built modules (excluding optional items) are available:
Order As LK83E (Tone Control Kit (mono)) Price £3.30
Order As LK84F (Tone Control Kit (stereo)) Price £5.75
Order As YM17T (Tone Control Module (mono)) Price £4.40
Order As YM18U (Tone Control Module (stereo)) Price £7.75

FILTER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,101	100k	2	(M100K)
R2,102	220k	2	(M220K)
R3,103	22k	2	(M22K)
R4,5,104,105	27k	4	(M27K)
R6,106	3k3	2	(M3K3)
R7,107	4k7	2	(M4K7)
VR1,101	470k Pot Dual Log	2	(FX14Q)
VR2,102	10k Vertical Sub-min Preset	2	(WR71N)
CAPACITORS			
C1,5,101,105	1μF Axial Electrolytic 100V	4	(FB12N)
C2,102	10pF Ceramic	2	(WX44X)
C3,103	22μF Axial Electrolytic 25V	2	(FB30H)
C4,104	4μ7F Axial Electrolytic 100V	2	(FB18U)
C6,106	1n5F Polystyrene	2	(BX58N)
C7,107	2n2F Polystyrene	2	(BX60Q)
C8,108	3n3F Polystyrene	2	(BX62S)
C9,109	4n7F Polystyrene	2	(BX64U)
C10,1010	10μF Axial Electrolytic 63V	2	(FB23A)
C11,1011	47pF Polystyrene	2	(BX26D)
C12,1012	100pF Polystyrene	2	(BX28F)
C13,1013	150pF Polystyrene	2	(BX29G)
C14,1014	220pF Polystyrene	2	(BX30H)
SEMICONDUCTORS			
TR1,2,101,102	BC107B	4	(QB31J)
MISCELLANEOUS			
L1,L101	Filter Pot Core	2	(LR07H)
S1,2,3	Maka Wafer 1-pole 12-way	3	(FH83H)
	Maka Shaft	1	(FH46A)
	HQ Mixer PCB No.9	1	(LR24B)
	HQ Mixer PCB No.29	1	(LR42V)
	Veropin 2145	1 Pkt	(FL24B)
	Multi-core Screened 6-way	As req	(XR26D)
	Multi-core Screened 15-way	As req	(XR28F)
	Multi-core Screened 25-way	As req	(XR46A)
	Min. Screened	As req	(XR15R)

module (MXR 9). Alternatively, it may be necessary for the user to have permanent control of the filter gain, and VR2/102 could be replaced by single or dual 10k potentiometers brought out into a more accessible position.

The filter select switch is bypassed or 'FLAT' in position 1 and the 'ROLLOFF' control VR1 has no effect. Succeeding positions of the rotary switch select ranges 15kHz to 5kHz which are the −6dB break points of the filter (see Figure 16). The Rolloff control further increases the signal attenuation between −6dB and −18dB per octave as shown in Figure 11.

Kits and Modules

Some of the modules described here are available in kit and ready-built form. However please note that both the kits and the ready-built PCB's *do not* include off-board components.

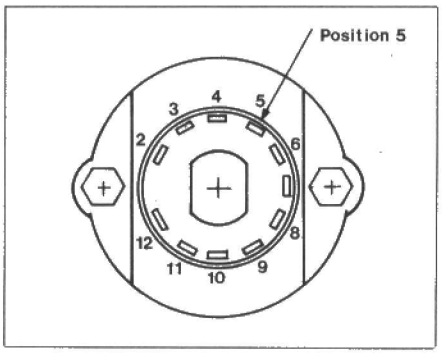


Figure 13. Locating Peg

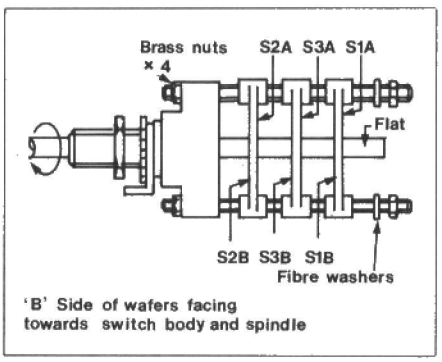


Figure 14. Assembled Wafer Switch

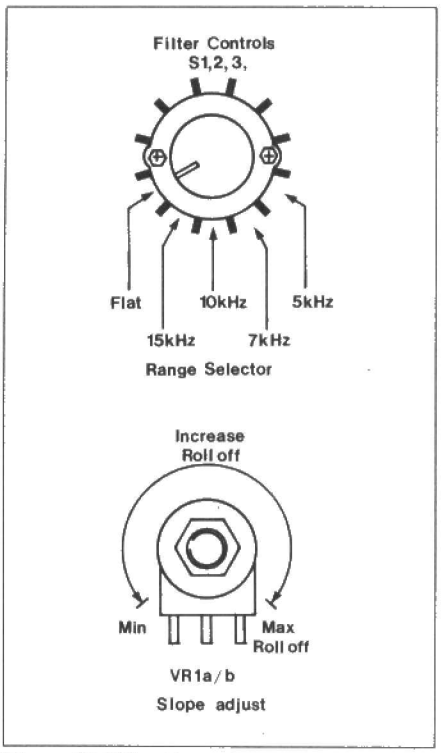


Figure 16. Filter Controls

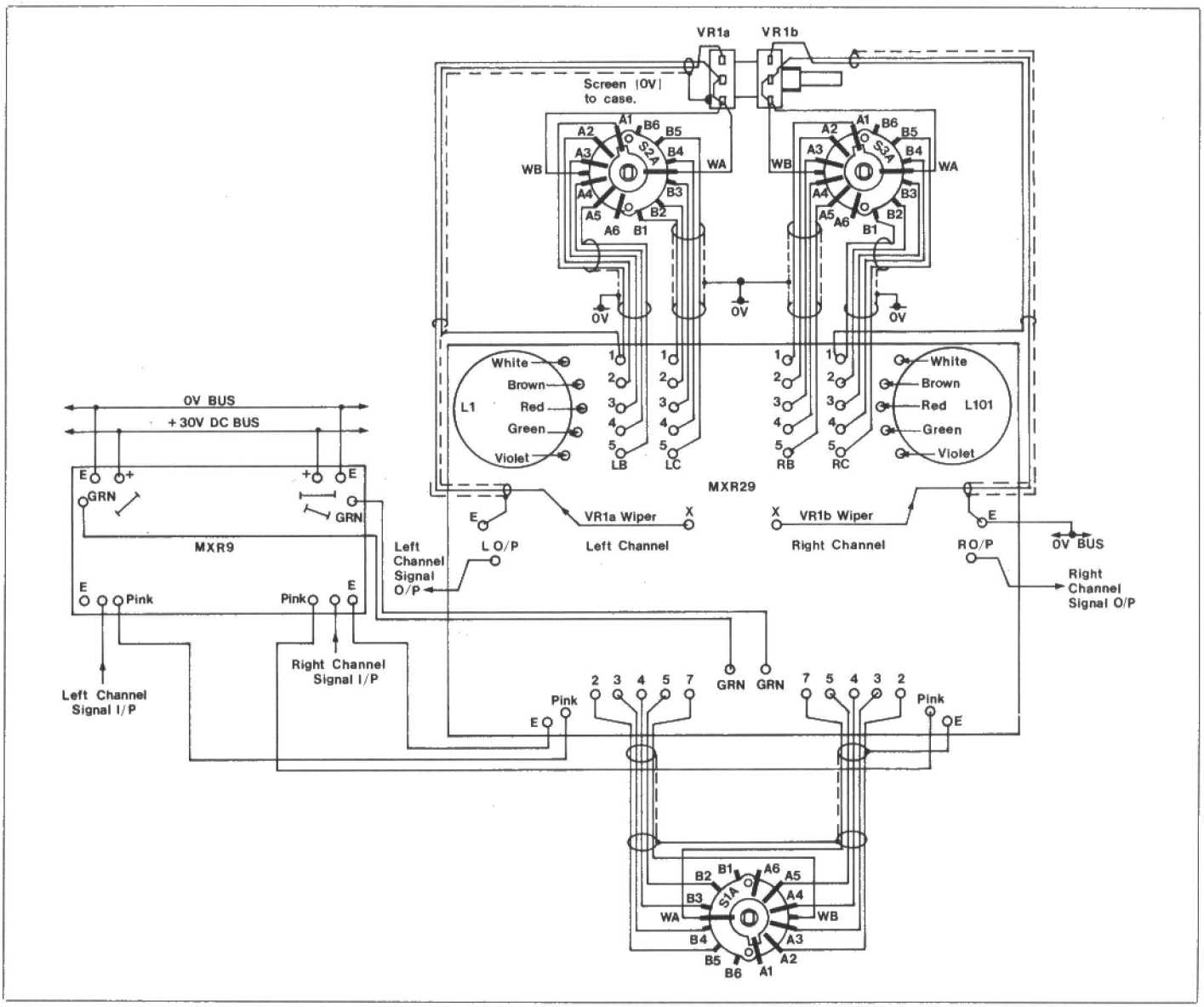


Figure 15. Interwiring

IBM GOLFBALL PRINTER DRIVER

by Paul Reeve **Part 2**

Part 2 of this project describes the functions of the driver card, and its construction. Its purpose is to interface the standard centronics interface available from most computers, to the solenoids and feedback contacts of the printer. These requirements are described below.

Centronics Requirements

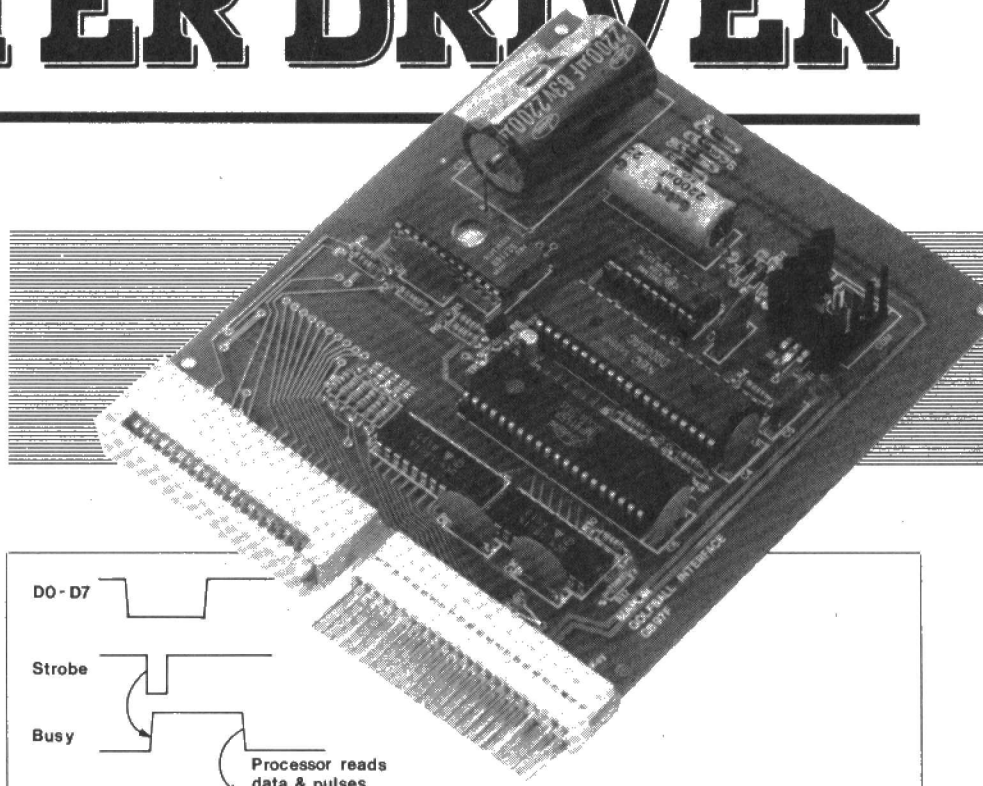
All centronics signals are TTL level compatible and the lines are described below in Table 1.

This concludes the test of 'active' lines used on this interface. The other lines are tied to 0V or 5V as required to allow normal operation, see Table 2.

The sequence of the active lines is shown in the timing diagram (Figure 1) and will be explained in conjunction with the timing of the printer signals.

Printer Requirements

The printer has seventeen solenoids which were shown in Figure 3 of Part 1, which are split into two groups T2, CHECK, T1, R2A, R1, R2 and −R5 form the character printer solenoids, whilst Shift Up, Shift Down, Ribbon Red, Ribbon Black, Tab, Space, Backspace, Linefeed and Carriage Return form the print function. These solenoids require a nominal 20 millisecond pulse of approximately 48V DC to activate the chosen printer function. Once a function has been activated, the feedback contacts give an idea as to the status of the cycle.



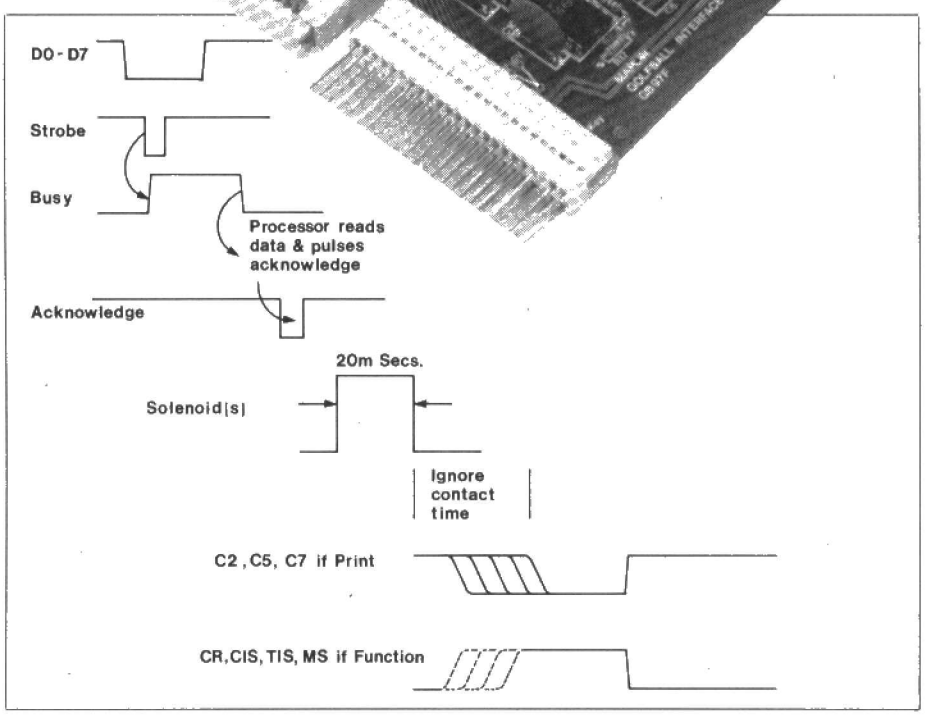


Figure 1. Timing Diagram

PIN	FUNCTION	
1	$\overline{\text{STROBE}}$	Signal goes low to tell printer to take the data presented at the 'data' inputs
2	DATA 0	
3	1	
4	2	
5	3	
6	4	
7	5	Data from computer
8	6	
9	7	
10	$\overline{\text{ACKNOWLEDGE}}$	A pulse low is given out from the printer to indicate that the data has been received and that another character can be sent
11	BUSY	A high given out from the printer tells the computer that it should not send any data yet.

Table 1

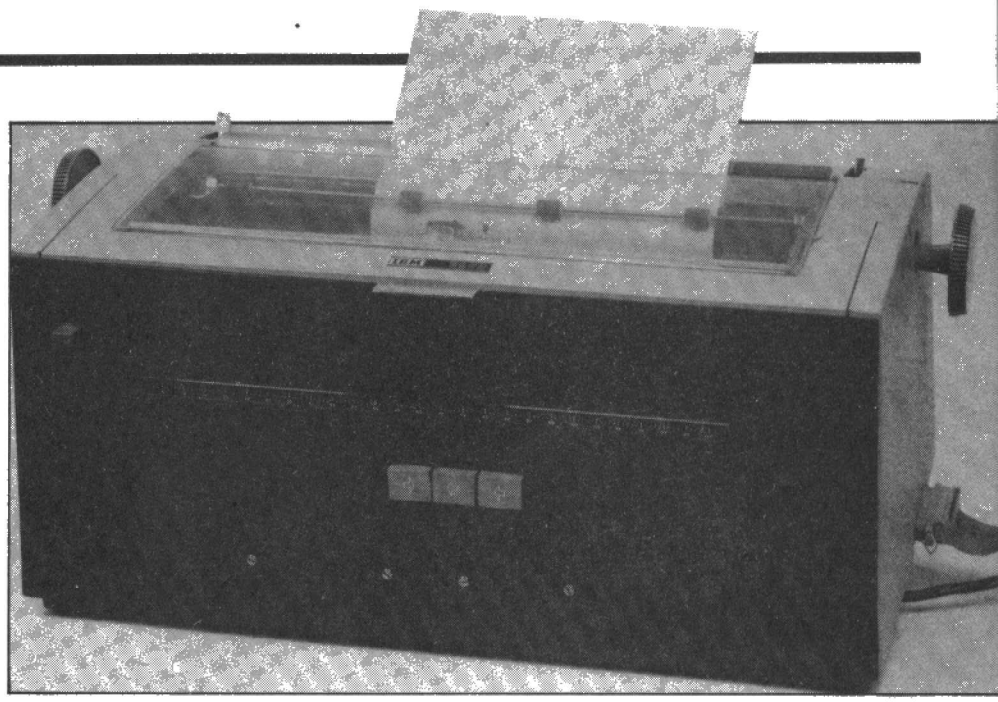
PIN	FUNCTION	
12	Paper Empty PE	0V
13	SELECT	Pulled to 5V
14	$\overline{\text{AUTO FEED}}$	See paragraph on Auto Feed
15	No connection	–
16	0V	0V
17	Chassis Ground	0V
18	NC	–
19-30	GND	0V
31	$\overline{\text{INIT}}$	Reset from computer
32	ERROR	Not used
33	0V	0V
34	NC	–
35	–	Pulled to 5V
36	SLCT IN	Not used

Table 2

	READ	WRITE
0000 to 07FF	2716	
0800 to 08FF	RAM	RAM
1800	8155 STATUS REGISTER	8155 COMMAND REGISTER
1801	PORT A	PORT A
1802	PORT B	PORT B
1803	PORT C	PORT C

These addresses are not unique as A13 – A15 are not used; therefore the map will exist at 8 locations throughout the 64K bytes of possible addresses.

Table 3



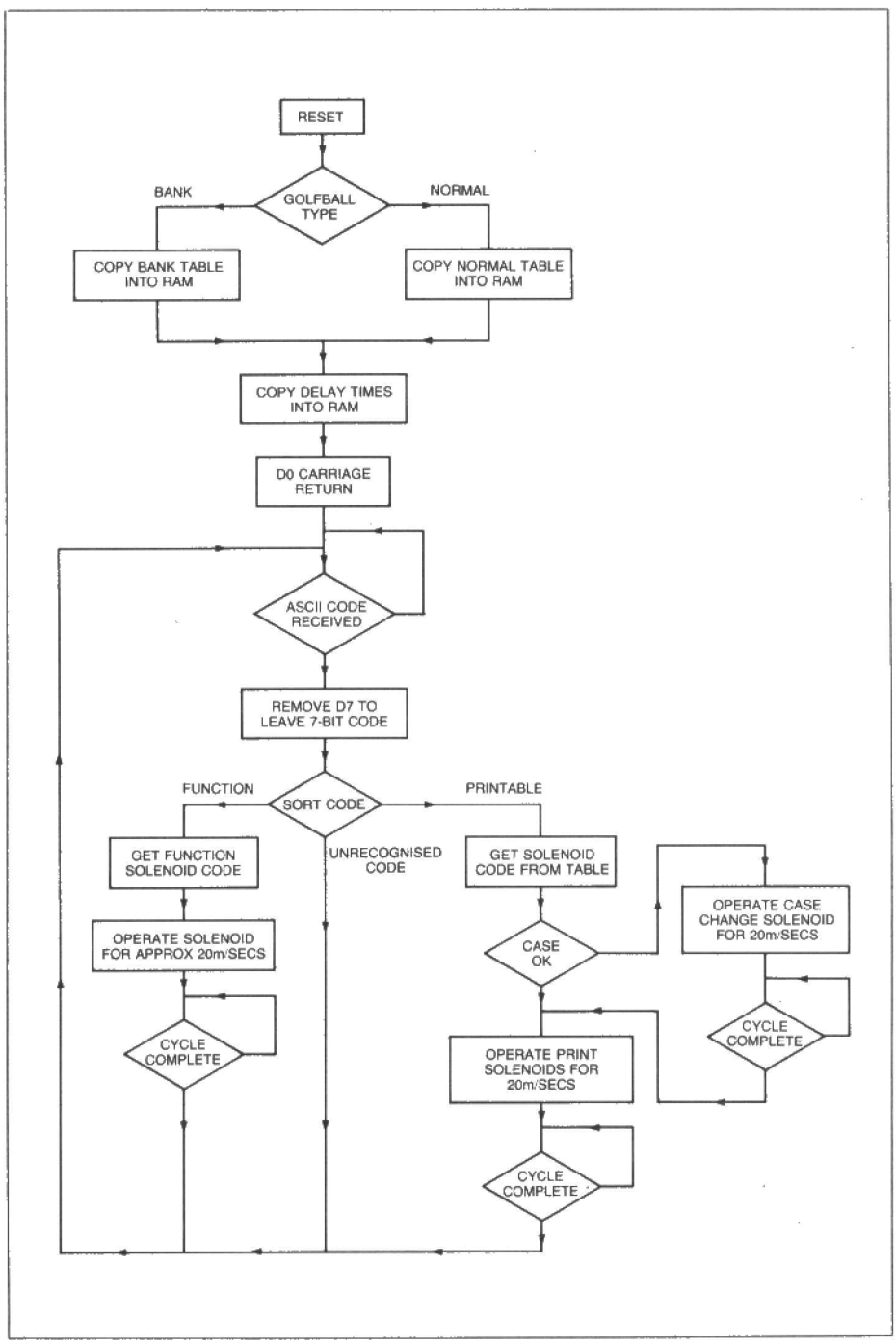


Figure 2. Program Flow Chart

The feedback contacts shown in the first part (CR, CIS, TIS & MS) were shown normally closed but they should have been shown as normally open. Grouping the contacts CR, CIS, TIS, & MS together with the large brown wire connected to the +5V and either the blue/brown or the white/orange wires pulled to 0V by a resistor on the circuit board, this would give a feedback for all of the print functions. A similar arrangement for CR, C5 & C7 will give the status of the character printing operation. This only leaves the last character contact which is used on itself.

Driving the Printer

These three lines are used to indicate the state of the printer and are best explained by the timing diagram.

To drive the printer, there are three obvious methods:

1. Use hard wired logic to produce the interface.
2. Use a microprocessor to do the same.
3. Use a driver program within the host computer to control the solenoids of the printer.

Method 3 is probably the most cost effective, but has the disadvantage of using part of the host computer memory which may exclude the use of long or multiple programs which require maximum memory space.

Method 1 is possible but would require such a large amount of logic chips that it becomes unpracticable. Hence method 2 is the one I have adopted.

The processor chosen is the 8085A because one of its support chips, the 8155 has a strobed input (port) with 2 lines that match the centronics requirements, these being strobe and busy which matches with the buffer full signal. The other active centronics line, 'ACKNOWLEDGE', is driven by the Serial Output Data (SOD) line of the microprocessor.

The switching of the solenoids is achieved by UCN5801A latching octal drivers which are capable of switching

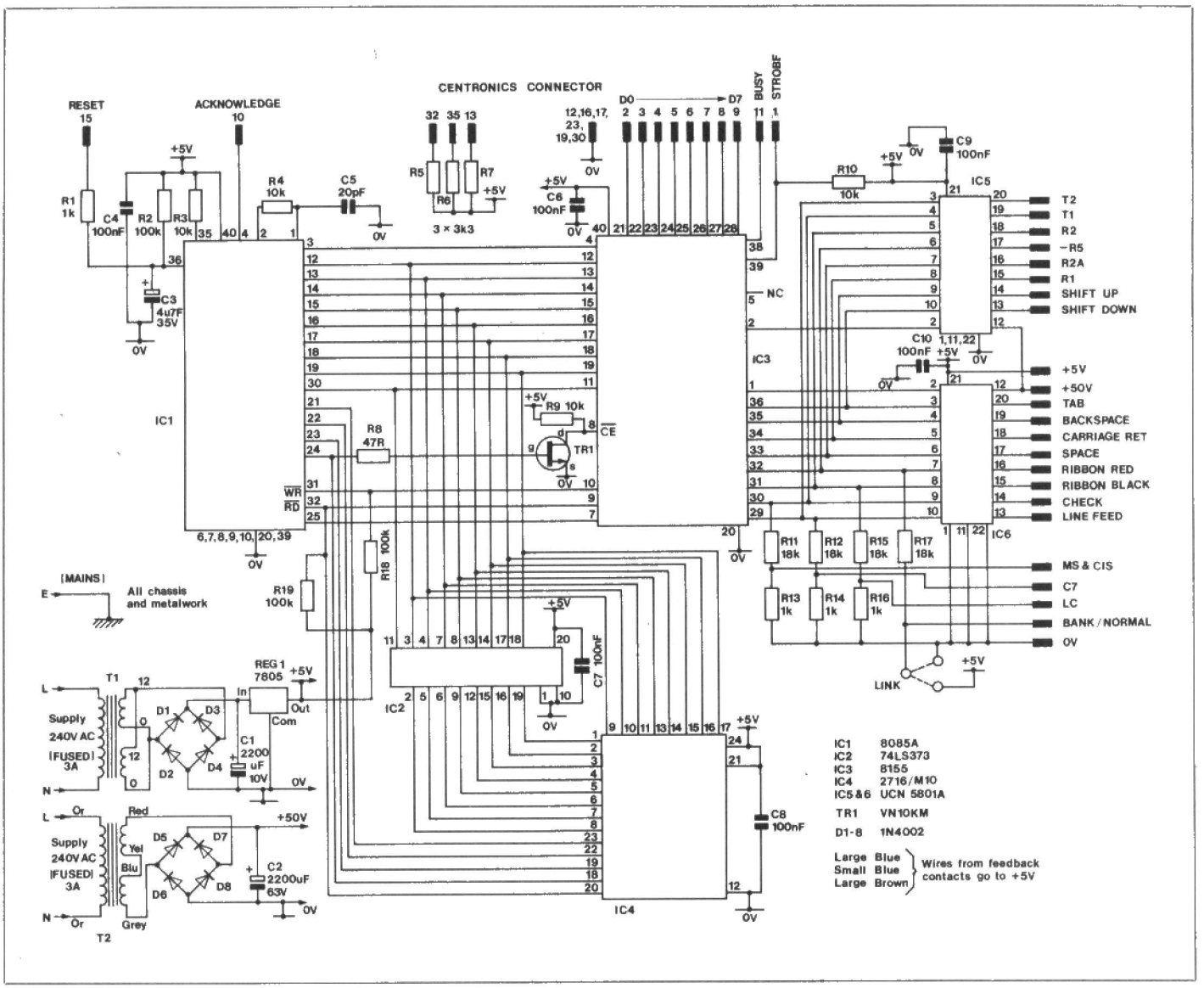


Figure 3. Circuit Diagram

the solenoids from a TTL level input. Two of these chips are used and they have a common data input supplied from Port B of the 8155 with the latches multiplexed by two of the lines from Port C.

Port B is also used as an input port to sample the three status lines during the appropriate part of the cycle. These input lines are connected via 18kΩ resistors in order to prevent these inputs pulling the port when it is used as an output. Being a support chip the 8155 connects very easily to the 8085A's multiplexed Address and Data busses, the only modification being the VN10KM transistor used on the CE line when A11 goes high. 256 bytes of RAM are also contained within the 8155.

Unfortunately, the ROM chip normally used with the 8085A is a high cost device, so a 2716 EPROM is used instead. This requires that the multiplexed address/data lines be latched by a 74LS373 to hold the lower 8-bits of the address. Table 3 shows the memory map of such a system.

Program Operation

Because the driver has to be able to cope with two types of golfball, the program contains two tables of data for solenoid combinations. Sampling the BANK/NORMAL line tells the driver which table to load into RAM. Obviously some users may have other golfballs with characters they require to be printed for certain ASCII codes, Table 6 gives details of memory locations and required changes to get an EPROM programmed for your own custom application.

LOWER CASE	80H
UPPER CASE	00H
ROW 0	03H
ROW 1	01H
ROW 2	02H
ROTATE 5	40H
ROTATE 4	20H
ROTATE 3	04H
ROTATE 2	24H
ROTATE 1	14H
ROTATE 0	08H
ROTATE -1	28H
ROTATE -2	0CH
ROTATE -3	2CH
ROTATE -4	1CH
ROTATE -5	3CH

e.g. Normal Golfball Character "V"
Coordinates = Upper Case, Row 2, Rotate -4

00H OR 02H OR 1CH = 1EH

Table 4

ADDRESS	FUNCTION	TIME (ms)
2D5H	CASE SHIFT PRINT	40
2D6H	CHARACTER	40
2D7H	SPACE	40
2D8H	BACKSPACE	40
2D9H	TAB	70
2DAH	LINE FEED	40
2DBH	CARRIAGE RETURN	70
2DCH	RIBBON COLOUR	60

Table 5

After this transfer, the timing variables are copied, these represent the time period during which the feedback contacts are ignored. This information is also given in the table. Lengthening the timing data will allow the printer to run without using the feedback contacts.

A carriage return is now performed and the driver then sets the golfball to lower case before waiting in a loop until a character is received. When a character is received, it is checked for being a

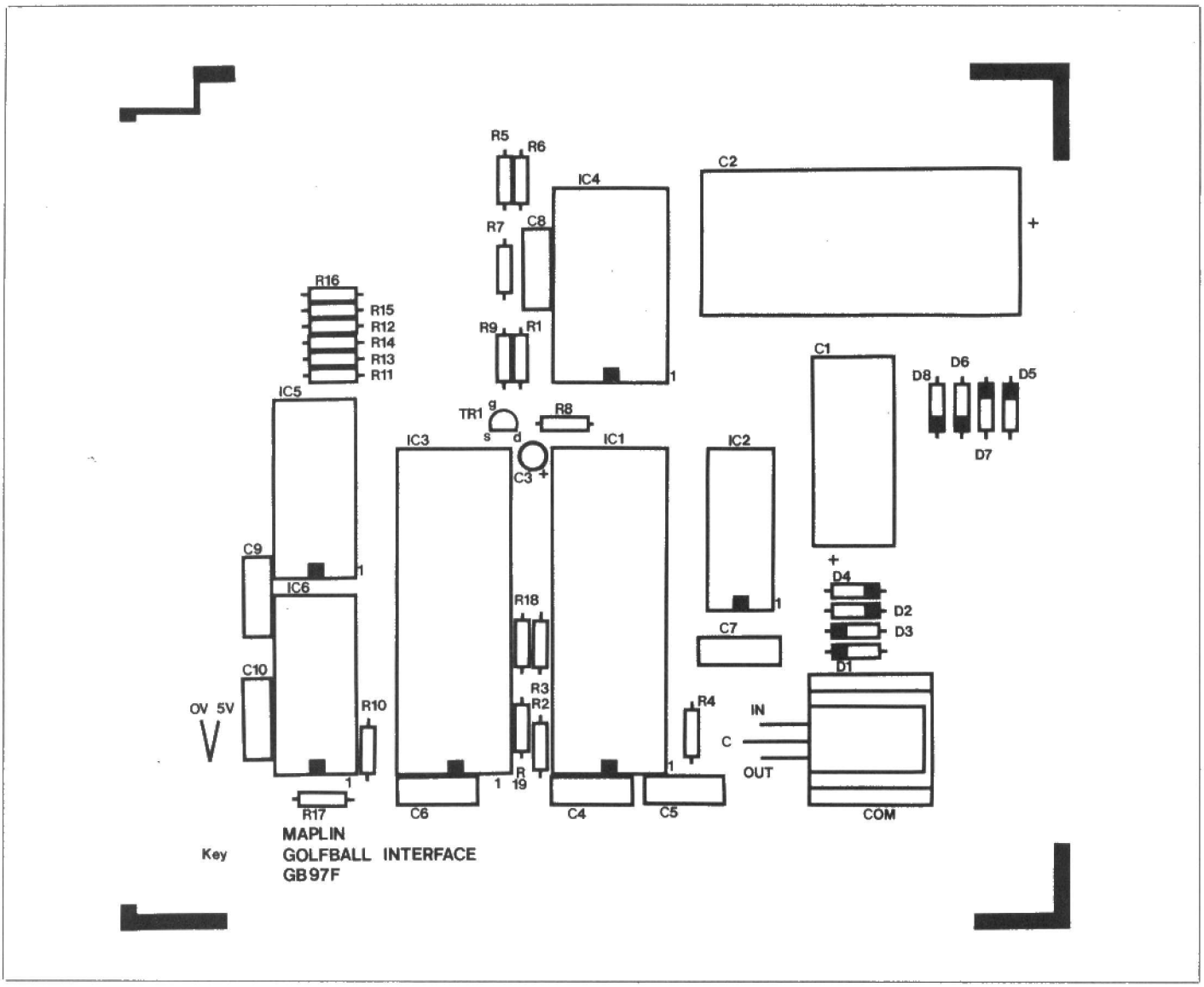


Figure 4. Printed Circuit Board Layout

printable character or a print function.

If it is printable the ASCII code is used to get the solenoid combination required from the earlier mentioned table. The case of the character is then checked before changing the golfball case to match (if necessary).

The code is then output for approximately 20 milliseconds, after which the 'ignore contacts' time is allowed to pass before the feedback contacts are monitored.

After this stage, the program loops back to wait for the next character, as you can see in the Flow Chart (Figure 2.)

Character Sets

The characters available on the two types of golfball have been assigned to the ASCII codes shown in the table. Should you wish to use this table you calculate the required byte by finding the location on the golfball. Give the co-ordinates of this point in terms of case, row and column (rotate), then using the values in Table 4 find the logical 'OR' of this combination.

The ASCII code for 'V' is 86_{10} = 56H, for NORMAL golfball selection add 1F5H, for BANK golfball selection add 255H, to give the locations in the EPROM where these characters are to be found.

Two other codes which can be stored in this table are 00H which will print a space or FFH which will be ignored, codes below 20H are unchangeable as they are PRINT functions which are handled elsewhere in the program.

The ribbon colour changes have been assigned to ASCII codes 18_{10} and 20_{10}.

Timing

The 'ignore feedback contacts' lines are stored at the locations shown in Table 5 with the values indicated.

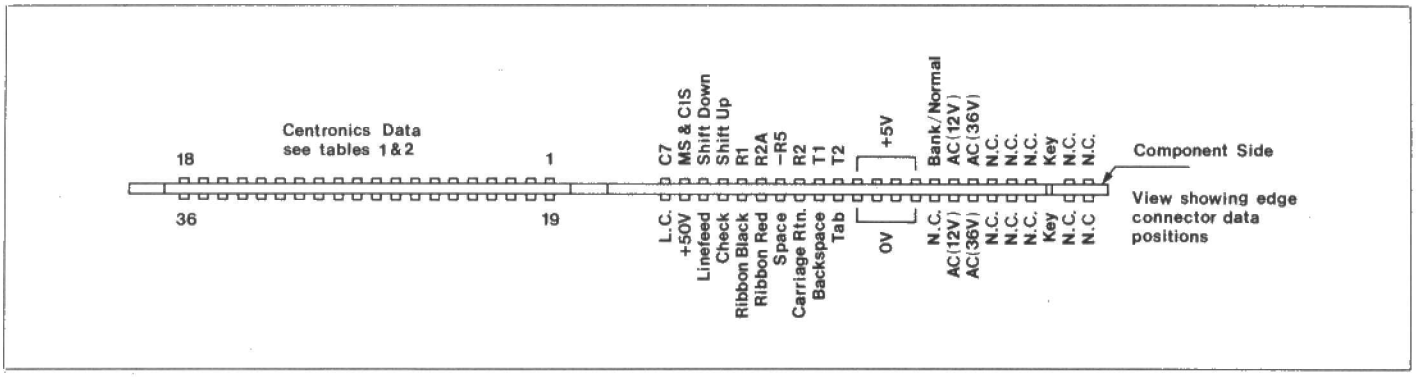


Figure 5. Edge Connector Pin-outs

ASCII Code(10)	NORMAL	CO-ORDINATE OR COMMENT	BANK	CO-ORDINATES	ASCII Code (10)	NORMAL	CO-ORDINATE OR COMMENT	BANK	CO-ORDINATES
32	SPACE		SPACE		79	O	U R2 C−1	O	U R3 C3
33	!	U R2 C0	!	U R0 C−1	80	P	U R3 C2	P	U R2 C−2
34	"	U R2 C2	"	U R1 C0	81	Q	U R3 C3	Q	U R0 C2
35	£	U RO C2	£	L R0 C1	82	R	U R2 C−3	R	U R2 C4
36	$	U RO C3	$	L R1 C3	83	S	U R2 C4	S	U R0 C1
37	%	U R3 C−1	%	U R1 C−2	84	T	U R1 C0	T	U R1 C−4
38	&	U R0 C−3	&	U R3 C0	85	U	U R1 C−4	U	U R1 C2
39	'	L R2 C2	'	U R0 C0	86	V	U R2 C−4	V	U R1 C−3
40	(	U R0 C5	(	U R3 C−5	87	W	U R2 C5	W	U R1 C3
41	)	U R0 C4	)	U R2 C−5	88	X	U R1 C−5	X	U R0 C5
42	★	U R0 C1	★	L R0 C2	89	Y	U R3 C4	Y	U R1 C−1
43	+	U R0 C−5	+	U R2 C5	90	Z	U R0 C0	Z	U R1 C4
44	,	L R3 C−2	,	U R0 C4	91				
45	−	L R3 C5	−	U R2 C0	92				
46	.	U R2 C1	.	U RO C−3	93				
47	/	U R0 C−4	/	U R1 C−5	94				
48	0	L R0 C4	0	L R2 C2	95	-	U R3 C5	-	U R3 C5
49	1	L R0 C−5	1	L R0 C4	96	'	L R2 C2	'	U R0 C0
50	2	L R0 C1	2	L R0 C−3	97	a	L R2 C−2	A	U R0 C3
51	3	L R0 C−4	3	L R1 C−5	98	b	L R1 C5	B	U R3 C1
52	4	L R0 C−1	4	L R2 C1	99	c	L R1 C−2	C	U R2 C−4
53	5	L R0 C2	5	L R3 C−4	100	d	L R1 C−3	D	U R3 C2
54	6	L R0 C3	6	L R2 C−1	101	e	L R1 C2	E	U R3 C−3
55	7	L R0 C−3	7	L R3 C4	102	f	L R3 C−4	F	U R2 C3
56	8	L R0 C−2	8	L R3 C3	103	g	L R3 C−5	G	U R3 C−2
57	9	L R0 C5	9	L R2 C−2	104	h	L R1 C4	H	U R3 C−1
58	:	U R3 C−3	:	U RO C−4	105	i	L R2 C3	I	U R3 C4
59	;	L R3 C−3	;	U R1 C1	106	j	L R3 C0	J	U RO C−2
60					107	k	L R1 C3	K	U R2 C1
61	=	L R3 C1	=	L R0 C5	108	l	L R1 C−1	L	U R3 C−4
62					109	m	L R2 C−5	M	U R2 C2
63	?	U R3 C1	?	U R2 C−1	110	n	L R1 C1	N	U R2 C−3
64	@	U R0 C−1	@	L R0 C−1	111	o	L R2 C−1	O	U R3 C3
65	A	U R2 C−2	A	U R0 C3	112	p	L R3 C2	P	U R2 C−2
66	B	U R1 C5	B	U R3 C1	113	q	L R3 C3	Q	U R0 C2
67	C	U R1 C−2	C	U R2 C−4	114	r	L R2 C−3	R	U R2 C4
68	D	U R1 C−3	D	U R3 C2	115	s	L R2 C4	S	U RO C1
69	E	U R1 C2	E	U R3 C−3	116	t	L R1 C0	T	U R1 C−4
70	F	U R3 C−4	F	U R2 C3	117	u	L R1 C−4	U	U R1 C2
71	G	U R3 C−5	G	U R2 C−2	118	v	L R2 C−4	V	U R1 C−3
72	H	U R1 C4	H	U R3 C−1	119	w	L R2 C5	W	U R1 C3
73	I	U R2 C3	I	U R3 C4	120	x	L R1 C−5	X	U R0 C5
74	J	U R3 C0	J	U R0 C−2	121	y	L R3 C4	Y	U R1 C−1
75	K	U R1 C3	K	U R2 C1	122	z	L R0 C0	Z	U R1 C4
76	L	U R1 C1	L	U R3 C−4	123				
77	M	U R2 C−5	M	U R2 C2	124				
78	N	U R1 C1	N	U R2 C−3	125				
					126				
Refer to Figure 26 of last issue. Format = Case, Row, Column (Rotate)					127				

Table 6. Golfball Locations of Characters

GOLFBALL PRINTER INTERFACE PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,13,14,16	1k	4	(M1K)
R2,18,19	100k	3	(M100K)
R3,4,9,10	10k	4	(M10K)
R5,6,7	3k3	3	(M3K3)
R8	47R	1	(M47R)
R11,12,15,17	18k	4	(M18K)
CAPACITORS			
C1	2200μF 10V Axial Electrolytic	1	(FB89W)
C2	2200μF 63V Axial Electrolytic	1	(FB92A)
C3	4μ7F Minelect	1	(YY33L)
C4,6,7,8,9,10	100nF Disc Ceramic	6	(BX03D)
C5	22pF Mica	1	(WX05F)
SEMICONDUCTORS			
D1-8	1N4002	8	(QL74R)
REG1	μA7805UC	1	(QL31J)
TR1	VN10KM	1	(QQ27E)
IC1	8085A	1	(YH41C)
IC2	74LS373	1	(YH15R)
IC3	8155	1	(QY80B)
IC4	2716/M10	1	(RA98G)
IC5,6	UCN5801A	2	(QY77J)

MISCELLANEOUS			
T1	Min. Tr 12V	1	(WB10L)
T2	Toroidal 30VA 18V	1	(YK12N)
	Golfball Printer I/F PCB	1	(GB97F)
	Vaned Heatsink	1	(FL58N)
	Col. Coded IDC Cable 40-Way	1 Mtr	(XR84F)
	40-Way IDC Edgeconn	1	(FT90X)
	PC Edgconn 2x23-way	1	(RK35Q)
	DIL Socket 20-Pin	1	(HQ77J)
	DIL Socket 24-Pin	1	(BL20W)
	DIL Socket 40-Pin	2	(HQ38R)
	Bolt 6BA x ½in.	1 Pkt	(BF06G)
	Nut 6BA	1 Pkt	(BF18U)
OPTIONAL			
	36-W IDC Centronics Chassis Skt	1	(FT74R)
	36-W IDC Centronics Plug	1	(FJ62S)
	Ribbon Cable 30-Way	1 Mtr	(XR67X)

The following items in the above list are available separately, but are not shown in the 1986 catalogue:

Golfball Printer I/F PCB **Order As GB97F Price £19.95**
Programmed Eprom 2716/M10 **Order As RA98G Price £9.95**
I/O Ports, RAM and Timer IC 8155 **Order As QY80B £1.95**

The time constant represents the multiplier for a delay loop which has a length of approximately the number of milliseconds delay required, dependant on the accuracy of the R & C combination used for the system clock. If your feedback contacts are not up to standard you can increase the values by getting the constant changed. To accommodate other frequencies, a byte in the EPROM can be adjusted. This is stored at address 206H, and is used to divide the clock frequency by n x 14_{10} to give a 1kHz value, where n is the number stored at address 206H. The initial value is 80_{10}, which corresponds to 80 x 14 x 1kHz = 1.12MHz which should allow for the spread of frequencies obtained by using an R/C clock.

Construction

The PCB and other components for the interface should all mount onto an aluminium plate, details of which are shown in Figure 6.

Assemble the power supply components first and check these out. Two transformers are used to prevent current surges from the solenoid drivers producing voltage transients along the 0V rail of the processor. For this reason, the 0V rails of both PSU's are linked via very thick PCB tracks at the UCN5801A's. After checking the supplies, discharge the capacitors with a 1kΩ resistor. Fig 7.

Add all the other components starting with the resistors, capacitors and then IC sockets. Carefully insert all IC's except the two UCN5801A's into their sockets. Using the edge connector diagram (Figure 5), wire up to the printer. Power up the 5V rail only. If all appears O.K., turn off and connect to your centronics socket to the PCB with the ribbon cable. Turn the unit on and the board will try to produce a carriage return.

If the processor is running you will be able to send characters without your computer locking up. If all is fine, install the 5801's and finish wiring the PCB into the printer, which should then function.

The 5801 IC's are soldered in position in the PCB, do this carefully with a low temperature iron and solder the earthed pins (0V) first. These IC's are power MOS devices so some care in handling is required – to help eliminate static charges attach a test lead with crocodile clips from the stem of the iron to 0V at the PCB, only whilst installing the 5801 IC's – they are soldered in this way in order to have a close thermal contact with the PCB tracks for heatsinking purposes.

Stickiness in the mechanism of the printer may cause problems with the spacing between characters, but this should improve with use. Care should be taken when wiring and connecting the 50V power supply because the solenoids and 5801 octal drivers are *only* specified to 50V. If you use a 34VAC rms output transformer, this will give a peak of ($\sqrt{2}$ x 34V) – (2 x 0.6) ≃47V, this may rise when off-load, causing concern for the expensive driver IC's. The prototype printer has been running for over 1 year with a 40V transformer without destroying any chips. Experiments have also shown that a 30V one will suffice with some printers.

This voltage can also destroy the other chips if it is allowed to appear in other areas of the PCB where it is not supposed to be – so be sure to discharge the reservoir capacitors using a resistor (≃500kΩ) before working on the circuit.

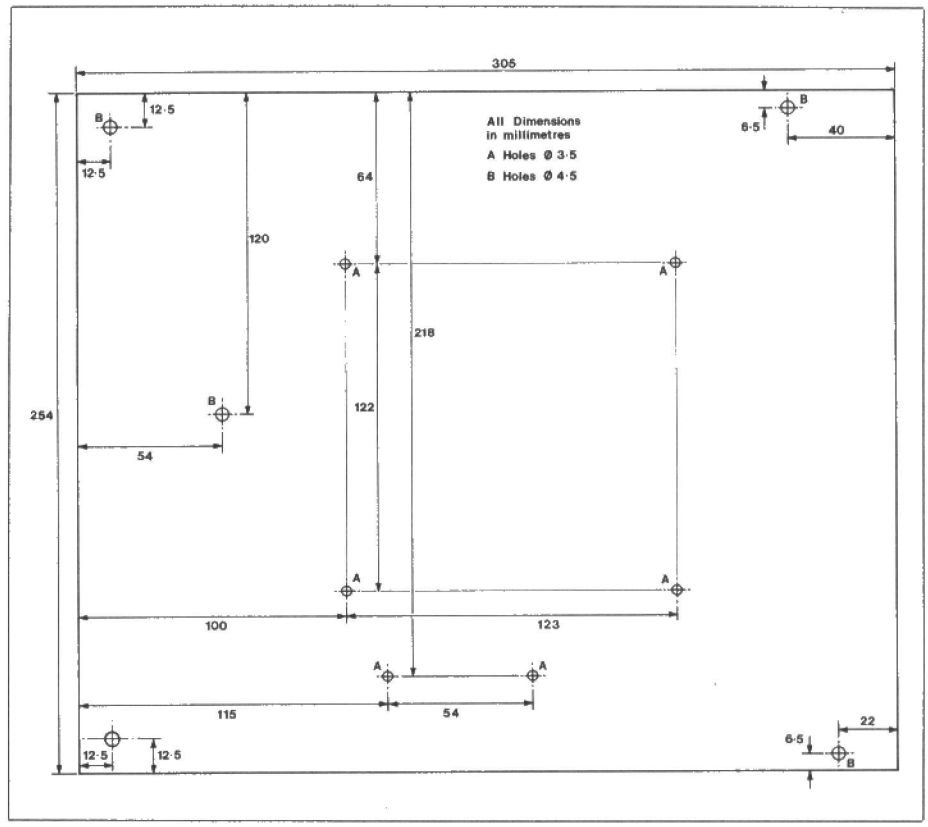
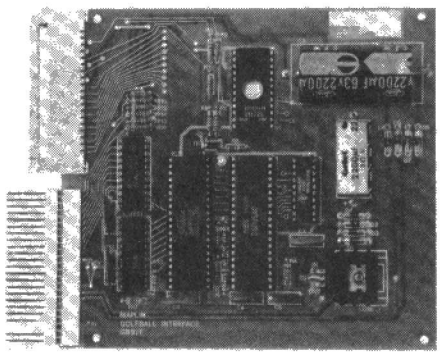


Figure 6. Suggested Mounting Plate Details



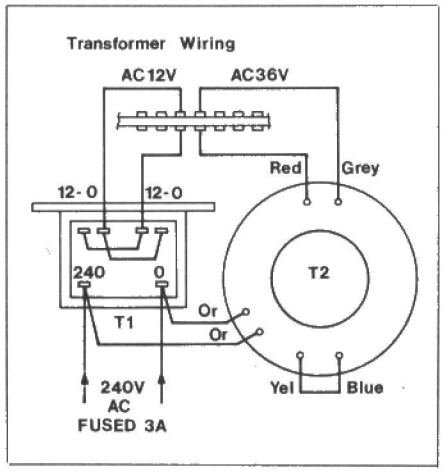


Figure 7. PSU Wiring

Power Up

Wire all of the mains leads to the printer's junction box. Then with your computer disconnected, switch on the printer; if all is well, the printer will do a linefeed and carriage return and the print head will rotate to the lower case position. The behaviour of the printer is unpredictable for the first few seconds until the processor has reset, so do not panic if it hammers away. If you have no success, wire in a reset button allowing a manual reset without power down, pushing this button should give the carriage return seconds after release. This manual reset is accessible at pin 15.

Careful soldering and wiring are a must with this project because fault finding a very difficult without an expensive emulator, logic analyzer or similar. Because of this, it is worthwhile spending several hours checking the solenoids work and the feedback contacts produce the required signals and I would like to thank a colleague Harry Jackson for his efforts on this and other tasks on the original prototype.

Auto Feed

Some printers produce a <CR> <LF> sequence to start a new line, whilst for others a <CR> only is used. These two combinations are accounted for by checking the voltage on pin 5 of the 8085, if this is high the interface ignores the next character received. Therefore set this pin to 5V or 0V via a 10kΩ resistor as required. If your centronics output sets the 'Autofeed' pin then pull pin 5 of the 8085 to +5V with a 100kΩ resistor, and connect this junction to the 'autofeed' of the centronics connector.

The Story of Radio

Photographs supplied by The Marconi Co. Ltd.

Marconi with his apparatus for 'telegraphy without wires', 1896.

by Graham Dixey

C. Eng., M.I.E.R.E.

Part One – The Early Years

The name of Guglielmo Marconi is synonymous with the birth of wireless or, as we call it today, radio. Communications have always been one of man's obsessions from the times when a runner would be sent with news of a victory in battle or of impending disaster. Allied with the need to communicate under such circumstances was the question of speed. The human runner, the horse, the lit beacons on hillsides, the semaphore of Napoleonic times all represent stages in the quest for fast communications.

Marconi's patents for telegraphy using Hertzian waves was granted on 2nd June 1896

In the 19th century this culminated in the telegraph, communication across country by wires strung between poles. This was an astonishing leap in technology, of course, the speed now being that of the flow of a current in a cable. But it was vulnerable; wires can be cut or brought down by storm or other natural phenomena. And it was expensive to lay across the sea, though in the middle years of the 19th century, Brunel's Great Eastern laid the first successful submarine cable across the Atlantic Ocean.

While due credit must be given to Marconi for his pioneering work in the field of wireless, one must remember that most great innovations are not just the work of one man but are usually brought to a head by that man (or team) as a result of applying his own individual talents to the work of others. In this case, Marconi did not discover the presence of wireless waves; Heinrich Hertz had sent and received them across his laboratory in 1817, Robert Clerk Maxwell had predicted their existence as far back as 1864. What Marconi did was to confirm the results of both of these gentlemen, to form a basis for his own researches and, using the technology of the day, to push back the frontiers of science. This is akin to the Wright brothers, who did not invent the science of aerodynamics, but confirmed current knowledge of it and applied their engineering skills to producing a practicable lightweight aero engine, thus making flight possible.

Collier-Marr Telephone and Self-Restoring Coherer c.1900, as used by Marconi to receive the first ever transatlantic signal on 12th December 1901.

Marconi

Guglielmo Marconi was born in 1874 of a Scottish/Irish mother and an Italian father. His education had suffered because he travelled a great deal with his mother. Nonetheless, in spite of an undistinguished academic background, he conducted experiments on Hertzian waves in the attic of his parent's villa near Bologna in 1894. The means of generating these early wireless waves was to develop a high voltage across a spark gap by means of an induction coil, a principle still with us today in the internal combustion engine. However, nowadays we suppress the radiation that Marconi was at such great pains to produce!

In 1897 Marconi transmitted a signal nine miles across the Bristol Channel

In the early summer of 1895 he managed to transmit several yards across his attic laboratory using a pair of metal plates as the radiating elements. Progress was relatively rapid because by August of that year, he had managed to increase the distance to one and threequarter miles. However, there was now another factor to consider in achieving this result.

There is obviously little point in being able to transmit a wireless wave unless there is also some way of receiving it. Hertz had proved the ability of wireless waves to communicate by causing a sympathetic spark to jump across the gap in his resonator (see Figure 1). However, this lacked sensitivity and was rather a dead-end line of enquiry. What Marconi used was a much more practical type of detector, known as a coherer.

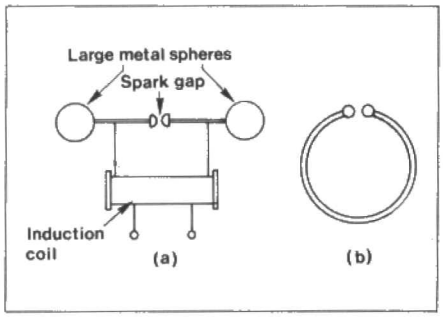


Figure 1. Hertz' original apparatus for sending and receiving wireless waves,
(a) his transmitter, using an induction coil to develop a high voltage across a spark-gap, which then broke down to radiate electromagnetic energy,
(b) his receiver, based on a resonator, which responded to the received energy and produced a weak spark in sympathy across a small spark-gap.

The Coherer

The coherer in the form in which Marconi used it was due to Sir Oliver Lodge, who had improved a similar detector, designed by the Frenchman Edouard Branly in 1890, and used it to transmit morse code over a distance of several hundred yards in 1894. This ushered in 'wireless telegraphy' though so far the range was too short to be taken seriously.

The coherer consisted of a small evacuated glass tube in which were placed two silver plugs attached to platinum wire. The inner ends of the plugs were cut at an angle and set quite close together. In the gap between was a mixture of nickel and silver filings (see Figure 2). Because the filings were loosely packed they possessed a fairly high value of resistance but, when a wireless signal was received, they clung together, bringing a dramatic drop in the resistance value – and a change of resistance on receipt of a signal is a phenomenon that offers obvious possibilities of conversion into some recognisable output.

However, it was necessary to give the coherer a tap to return it to its high

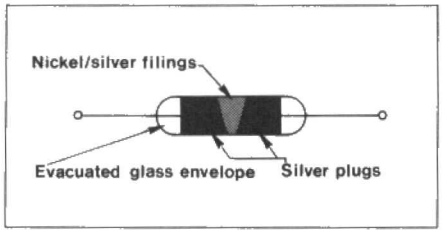


Figure 2. The basic form of Marconi's original coherer. The proportions of silver/nickel were varied to improve the sensitivity. The silver plugs gave a good ohmic contact with the filings.

Marconi , 1896.

resistance state before it would respond to the next signal impulse. In practice, the coherer was placed in series with a battery and a recording inker, so producing a pen trace of the signal; a bell could be included in the circuit so that its hammer could give the coherer the required tap (see Figure 3). Marconi spent much time improving the coherer's sensitivity by experimenting with the ratio of nickel to silver, ending up with a 19:1 ratio as being the optimum.

Essentially Marconi's transmitter was of the type used by Hertz, and the radiation efficiency of this system was improved by using large metal plates, one suspended in the air and the other set in the ground, giving birth to the idea of the aerial and earth system. A similar arrangement was used at the receiver.

So successful was the transmitter/receiver arrangement that Marconi now approached the Italian Ministry of Posts and Telegraphs who, with lamentable lack of foresight, turned down his offer. It was this rejection that caused Marconi to come to England, which he did in 1896. Here he received help from his cousin, Henry Jameson Davis, and filed a patent application for a system of telegraphy using Hertzian waves. British patent No. 12039 was granted on 2nd June 1896.

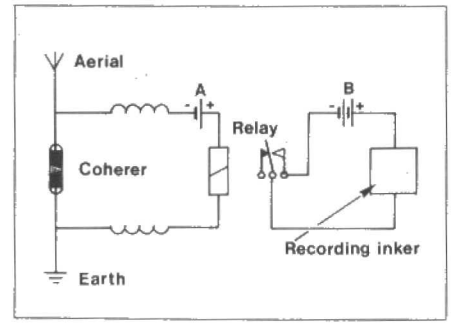
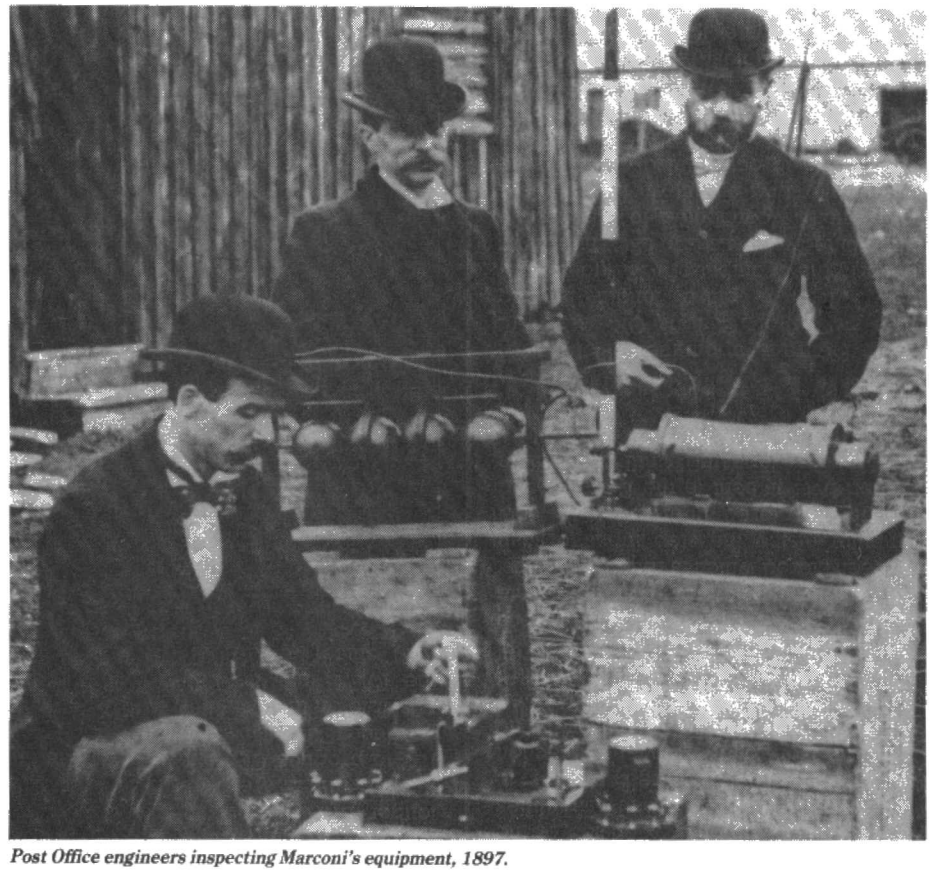


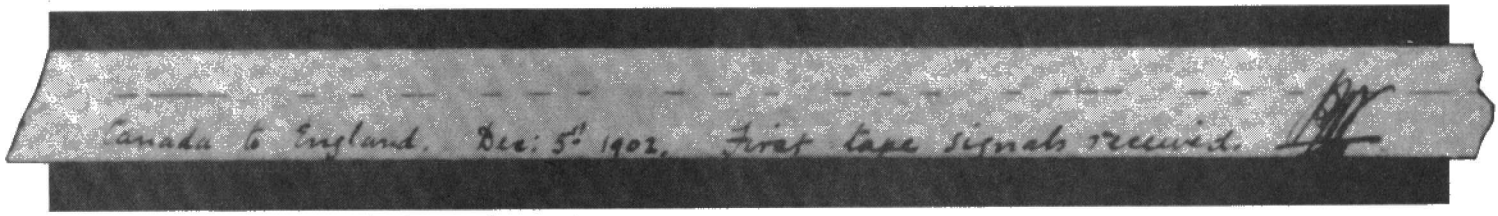
Figure 3. A receiver using a coherer. The reduction in resistance of the coherer when a signal was received caused the relay coil to be energised by battery A. The change-over contacts then energised the recording inker via battery B, so giving a visible mark on paper tape.

The English Connection

In England Marconi found enough people to take an interest in his work. One person he was introduced to was William Preece, Engineer-in-Chief of the Post Office. Preece was also experimenting with 'wireless communication', but using mutual induction between loops rather than spark



Post Office engineers inspecting Marconi's equipment, 1897.



The evidence – the first Transatlantic signals captured on paper tape.

transmission. After some initial laboratory demonstrations, Marconi was invited to give a demonstration to officials of the Post Office. The transmitter and receiver were set up on the roofs of two buildings a few hundred yards apart, in the city, and a successful demonstration took place. This impressed the officials considerably, especially as the signals had quite obviously cleared the intervening buildings. He was invited to participate in further tests.

These tests took place on Salisbury Plain in September 1896, and Marconi used both his conventional aerial and earth system *and* a parabolic reflector, thus demonstrating both short-wave line of sight transmission in addition to the possibility of obtaining directional beam effects with such transmissions.

Not only was the Post Office represented at these trials but there were representatives from the War Office and the Admiralty as well. The interest shown by the Navy is understandable since a reliable system of wireless communication was likely to be of inestimable value to ships at sea, that were otherwise quite isolated from contact with land once they had sailed. A further demonstration given by Marconi was for the benefit of the public and Press in London, when he walked around with a receiver incorporating a bell. Whenever Preece, who was up on the stage, pressed a button, the bell rang.

Marconi Triumphs!

In the summer of 1897 Marconi participated in further tests of great importance. It had to be proved that transmissions could take place over water, if wireless was to be used to replace, for example, submarine cables. These tests took place in the Bristol Channel and took the form of a direct comparison between Marconi's system and Preece's induction system. Both of them managed to bridge the gap to an island three miles offshore, but Marconi also managed to send a signal right across the nine mile width of the Channel. The question was, what to do next? The answer was quick in coming.

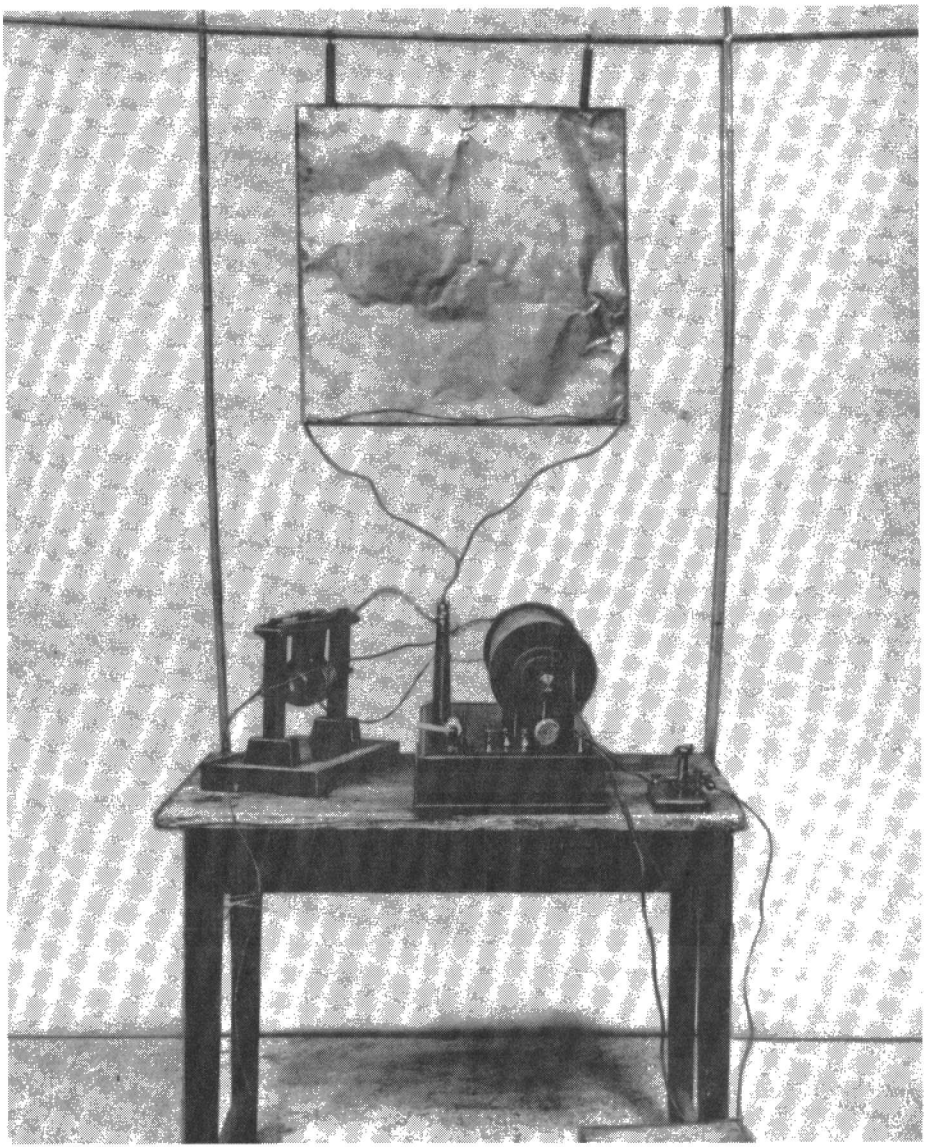
On 20th July 1897, 'The Wireless Telegraph and Signal Company Limited' was formed. Marconi now had to establish sites for the company to use. He chose two coastal sites, the Needles Hotel in Alum Bay on the Isle of Wight and the Haven Hotel in Poole, Dorset. These were about 18 miles apart. By November of that year, he had built a 120 foot high mast outside the Needles Hotel and was ready for some shore-ship tests. A small tug-boat was obtained and, in spite of some heavy weather, successful communication was achieved up to a distance of about 18 miles.

Rescue at Sea

The year 1898 saw some notable events taking place. Marconi, who had been spurned by his own government and had left Italy as an unknown, was now invited back and fêted. Not only this, but the Italian Navy adopted his equipment for use on their ships. Back in England, he set up an experimental station on the Goodwin lightship which communicated with the South Foreland lighthouse. This link proved useful in allowing a number of emergencies to be reported, one of which was the first rescue at sea by wireless, when the S.S. R.F. Matthews collided with the lightship! Other notable events included the setting up of a wireless link between Osborne House on the Isle of Wight and the Royal yacht in the Solent, so that Queen Victoria could communicate with the Prince of Wales.

Royal Patronage as a wireless link is set up in Osborne House so that Queen Victoria could communicate with Prince Albert on the Royal Yacht in the Solent

The following year, 1899, Marconi's newly founded company acquired premises in Hall Street, Chelmsford and so was built the world's first radio factory. The year 1899 was a notable one in the annals of wireless telegraphy. During this year, it took on an international flavour when a station was set up at Wimereux, near Boulogne, to communicate with the South Foreland Station. An interesting side issue grew out of this link. It happened that there was a meeting of the British Association at Dover at the same time that a similar type of meeting was taking place in Boulogne. A



A replica of Marconi's first transmitter used in Italy in 1894.

temporary mast was erected at Dover Town Hall to exchange messages, which worked well, so well in fact that these messages were also picked up at Chelmsford, over 80 miles away! Marconi had discovered the action of the ionised layers of the atmosphere in bending the radio waves back to earth, though it is doubtful if the full significance of this was appreciated at the time.

Also in 1899, W/T, to give it its abbreviated title, went to sea with the Royal Navy on manoeuvres and, due to a high degree of co-operation between Marconi and a naval officer, Captain Henry Jackson, RN, was a marked success. The South African War saw the use of W/T and, in a more peacful context, it crossed the Atlantic to report the progress of the America's Cup races. In November of the same year, The Marconi Wirelss Telegraph Company of America was registered, better known to us today as simply RCA.

We tend to think that the rapid growth of electronic technology is a modern phenomenon, but a moment's thought on what has been written so far will show that a mere five years had elapsed between Marconi's first test transmissions in his attic and the use of wireless as a practical means of communication.

Improvements in range had come about by developing the original circuit, not just by pushing up the input power. The most significant feature of the new transmitters and receivers was the use of radio-frequency transformers, known as 'jiggers'. In the transmitter, the spark gap was used to discharge a high value of capacitor (storing a large quantity of electrical energy) through the primary winding, the aerial being connected in the secondary circuit. In the receiver, the jigger was used as an impedance matching device between the aerial and the high impedance coherer. The use of these transformers allowed the incorporation of a facility that became more vital as W/T communications became more widespread and the 'radio band' more crowded – the need to make both the transmitter and receiver circuits 'resonant' at the same frequency, so as to avoid mutual interference between stations operating simultaneously; this frequency selective method of operation had been impossible initially.

Letter 'S' was the first transmission across the Atlantic

The year was now 1900 and the use of W/T was rapidly being adopted by a variety of services, especially at sea. This was the year in which the marconi International Marine Communication Company Limited was formed; it was also about the time that Marconi began thinking in terms of spanning the Atlantic with wireless waves.

Waves Across The Waves

In 1901, Marconi established communication between the Isle of Wight and the Lizard, a distance of almost 200 miles. At the same time, Marconi's team consisting of Vyvyan, Professor Fleming, Paget and Kemp began the construction of the eastern end of the transatlantic link, at Poldhu in Cornwall. Marconi himself crossed the Atlantic to see about setting up the other end of the chain at Cape Cod.

The weather, the enemy of so many pioneers in many fields, destroyed the aerial systems at both ends of the link. That at Poldhu, which had been on the lines of a vertical cylinder of conductors, was replaced by a fan-shaped design, while the station at Cape Cod was abandoned in favour of a new site at St. John's, Newfoundland. The aerial here was to be launched on a kite, a tricky operation in the high winds. Nonetheless, it was managed eventually and, on 12th December 1901, Marconi and Kemp both agreed that they could just make out the three dots of the morse letter 'S' against the background of static.

There are some significantly interesting technical details concerning the equipment used. Firstly, the system was untuned, unavoidably because the erratic behaviour of the kite aerial made it impossible to hold the receiver on one frequency. Secondly, Marconi was using what was called a 'self-restoring coherer' – which was not a coherer at all but a true r.f. detector, together with an earphone to give an audio output. Thus was the first trans-atlantic wireless contact made, from Poldhu in Cornwall to St. John's in Newfoundland, a distance of 2,099 miles!

There were sceptics, of course. After all, there was no physical evidence to show that the signal had actually been received. Perhaps Marconi and Kemp had both imagined it? To quieten the sceptics, two months later, on the liner S.S. Philadelphia, Marconi recorded signals, using the morse inker, which confirmed on paper tape the reception of the letter 'S' at a distance of 2,099 miles and a full message, which was readable, at distances up to 1,551 miles.

The age of wireless could be truly said to have arrived at that moment. It was now just a question of developing the new science. The following decades were to see some very exciting events as, in peace and war, the infant technology grew to full stature.

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Hobbyist's Temperature Controller

★ Temperature Range 13 to 27°C
★ Current Range upto 4 Amps
★ Wide Range of Applications

by D.E. Coe

Originally designed to control the temperature of a home-brew wine and beer fermentation cabinet, this unit provides a thermostat facility for a wide range of other activities; tropical fish aquaria, photographic processing and hot-house gardening to name but a few. In its described form, the unit covers an adjustable temperature range of 13–27°C (or 55–80°F) but modified ranges are easily accommodated.

The unit provides heating via an ordinary 60 watt mains light bulb or any other mains heating unit for which the turn-on surge current does not exceed 4 amps. Temperature sensing is performed with the LM334Z IC, the circuit of which is separated from the high voltage by the opto-isolator.

The LM334Z, realised in a 3-lead TO92 package, is designed primarily for use as a wide range adjustable current source. The current I_{SET} is determined according to Equation 1 where V_S is the device sense voltage and the adjusted resistor R_{SET} is between the V− and 'r' pins of the IC.

Equation 1

$$I_{SET} = \frac{V_S}{R_{SET}}$$

However, the linear temperature response of the sense voltage V_S makes it admirably suited for temperature sensing (Figure 1). The basic circuit, shown in Figure 2, gives an output potential change of 10mV/°C with the component values shown.

The Circuit

The circuit diagram is shown in Figure 3 and uses the CA3140E MOSFET input op-amp in a comparator configuration. The op-amp is used in a single rail arrangement at open loop gain and C1 improves HF stability. The voltage

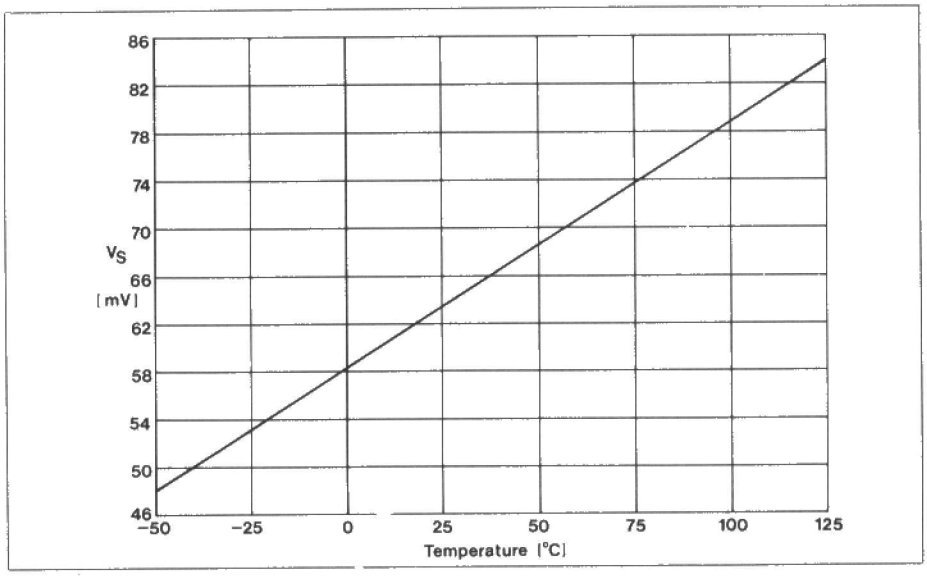
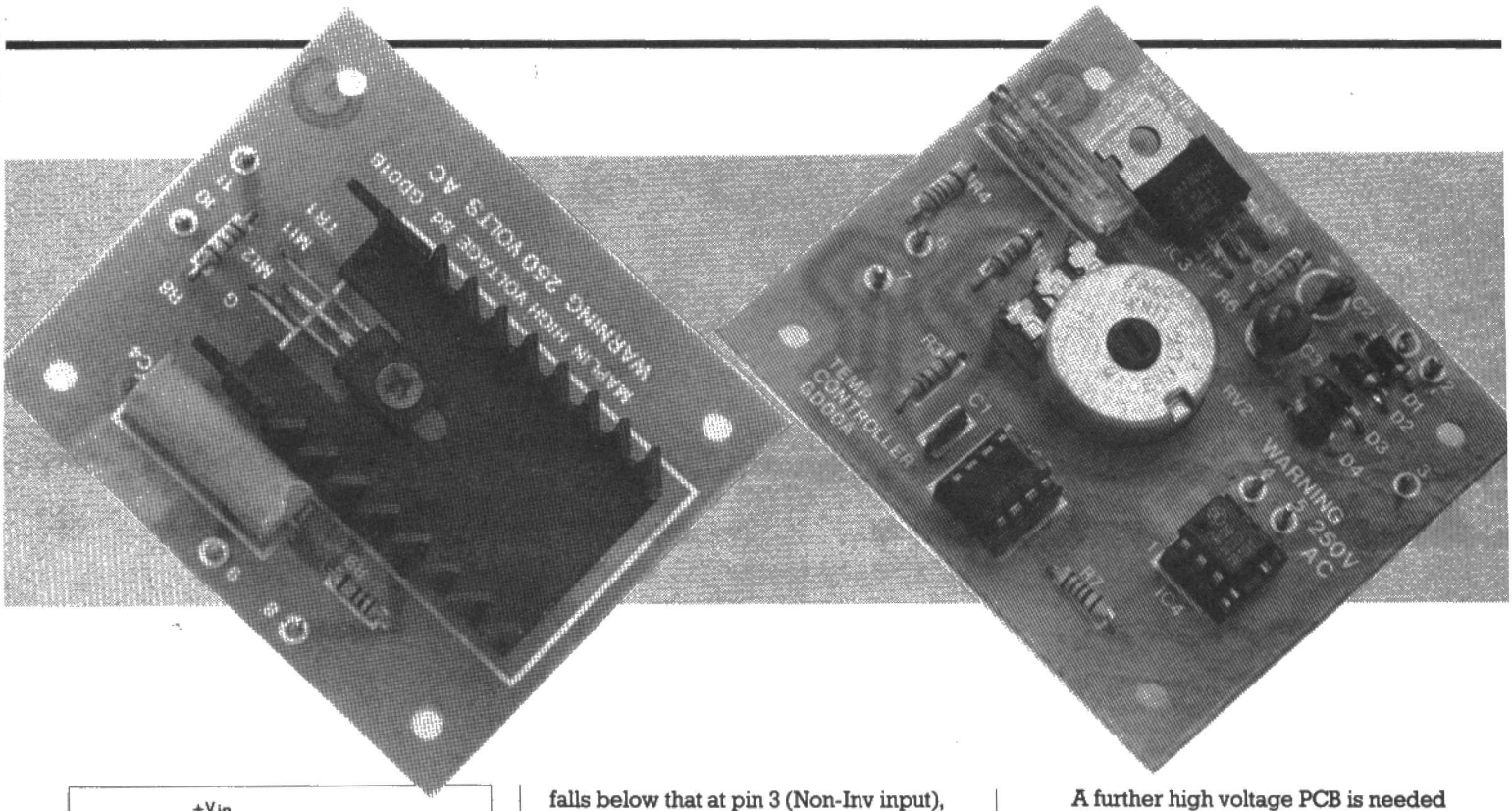


Figure 1. Temperature Response



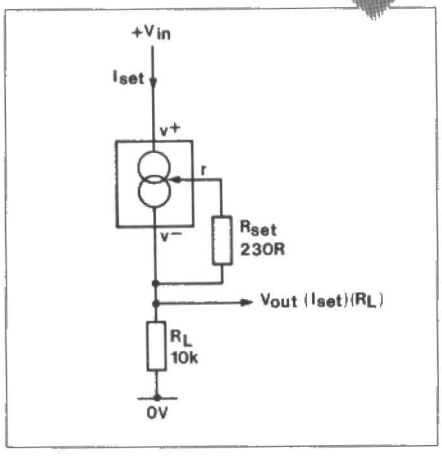


Figure 2. LM334Z Circuit

regulator IC3 provides both a regulated supply rail and acts as a reference voltage source for the op-amp Non-Inv input (pin 3) resistor chain.

As the sensor temperature falls, then so does the potential at pin 2 (Inv-input) of IC2 due to the change in sense voltage (V_S) of IC1. When the potential at pin 2 falls below that at pin 3 (Non-Inv input), set by RV2, the output which until then was close to the negative power rail will switch smartly to be close to the positive rail, thus turning on the LED of the opto-isolator.

Opto-isolation is provided via the opto-triac IC4, which is used to trigger the power triac TR1. By this means, the low voltage sensing circuitry is separated from the mains wiring. The capacitor-resistor combination of C4 and R9 form an interference suppression network to keep interference within acceptable limits.

Construction

As mains voltages are being handled scrupulous attention to all aspects of safety should be observed. An adequately earthed diecast box is suitable for housing the main circuitry. The printed circuit and overlay for the main PCB is shown in Figure 4. Construction is carried out with reference to the Parts List.

A further high voltage PCB is needed (Figure 5). It supports R8, the interference suppression components C4 and R9, and the power triac TR1 mounted on its heatsink.

Care should be taken to ensure correct polarity of diodes, electrolytic capacitors, integrated circuits and the opto-triac. Some useful pin-out diagrams are shown in Figure 6. Particular care should be taken when inserting the 6-pin DIL opto-triac package for both its orientation and correct pin positioning in the 8-pin DIL socket. The potentiometer RV2 should also be mounted correctly with the body on the component-side and spindle track-side of the circuit board (otherwise the temperature scale will be found to be reversed). A suitable scale for the potentiometer RV2 is shown in Figure 7.

Figure 8 shows the wiring diagram. The main circuit board and the high voltage PCB should be stacked with spacers ensuring that adequate clearances result all round between the high

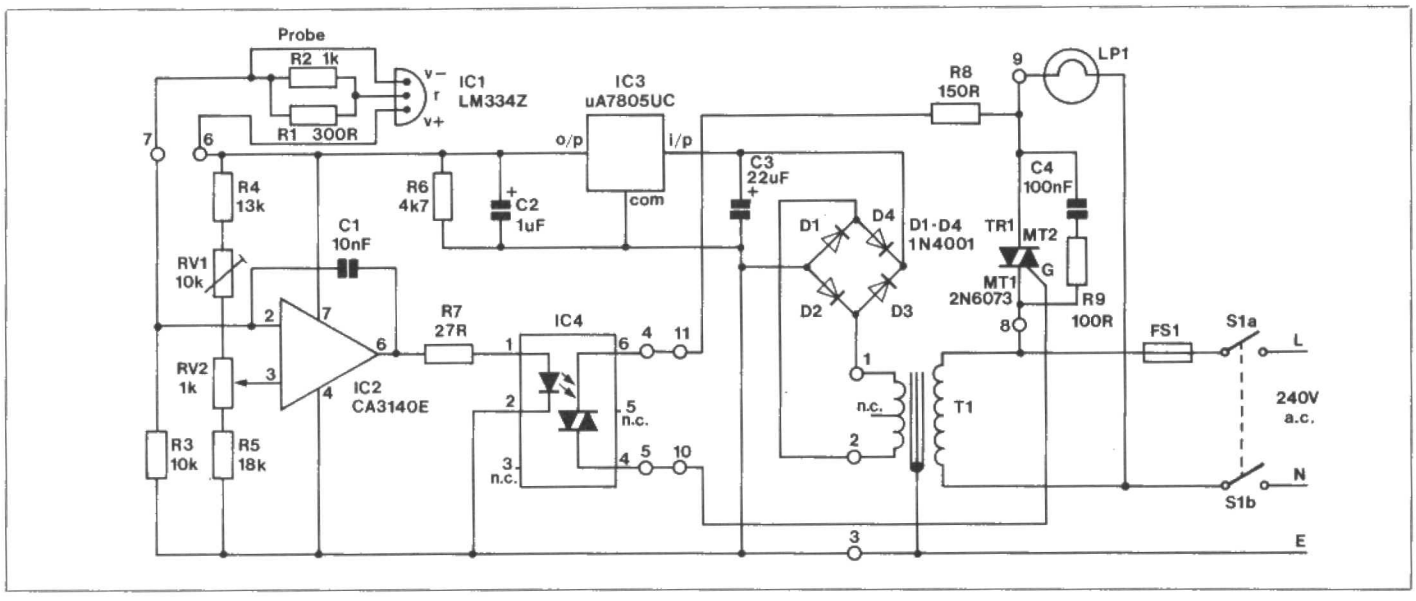


Figure 3. Temperature Controller Circuit

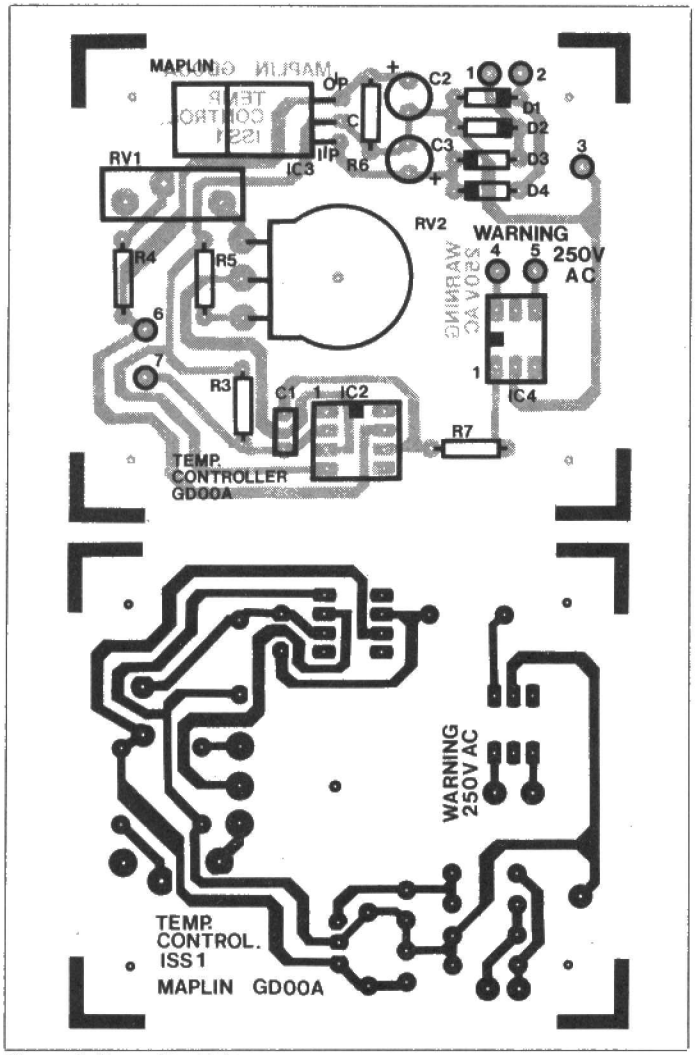


Figure 4. Controller PCB

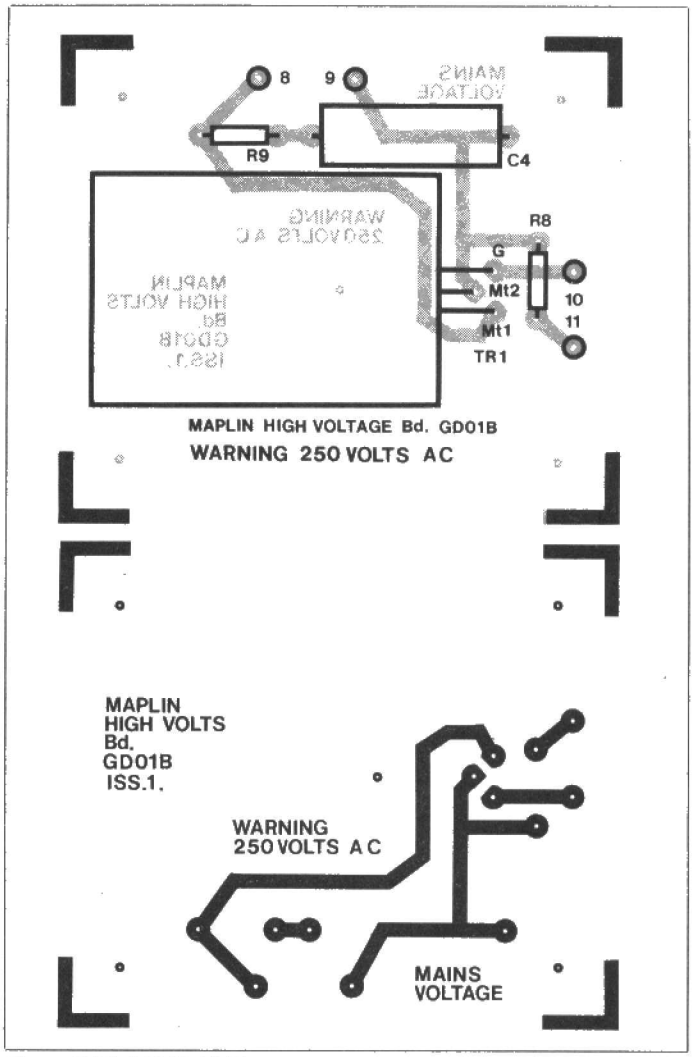


Figure 5. High Volts PCB

HOBBYISTS TEMPERATURE CONTROLLER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	300R	1	(M300R)
R2	1k	1	(M1K)
R3	10k	1	(M10K)
R4	13k	1	(M13K)
R5	18k	1	(M18K)
R6	4k7	1	(M4K7)
R7	27R	1	(M27R)
R8	150R	1	(M150R)
R9	100R	1	(M100R)
RV1	10k 23-Turn Cermet Preset	1	(WR49D)
RV2	1k Lin Pot	1	(FW00A)

CAPACITORS

C1	10nF Disc Ceramic	1	(BX00A)
C2	1μF 35V Tantalum	1	(WW60Q)
C3	22μF 25V Tantalum	1	(WW73Q)
C4	100nF Interference Suppression	1	(FF56L)

SEMICONDUCTORS

D1,2,3,4	1N4001	4	(QL73Q)
IC1	LM334	1	(WQ32K)
IC2	CA3140E	1	(QH29G)
IC3	μA7805UC	1	(QL31J)
TR1	2N6073	1	(QR51F)
IC4	Opto-Triac Isolator	1	(QQ10L)

MISCELLANEOUS

S1	Dual Rocker Neon Switch	1	(YR70M)
T1	Sub-Min Transformer 6V	1	(WB00A)
FS1	2A 20mm Fuse	1	(WR05F)
	20mm Fuseholder	1	(RX96E)
	8 pin DIL Socket	2	(BL17T)
	Control Knob	1	(FK41C)
	Temp Control PCB	1	(GD00A)
	Strain Relief Grommet	2	(LR47B)
	High Volts PCB	1	(GD01B)
	Stick-on Front Panel	1	(FA85G)
	Heatsink	1	(FG83H)
	6BA C/S Screw x ¼in.	1 Pkt	(LR56L)
	6BA Nut	2 Pkts	(BF18U)
	6BA Solder Tag	1 Pkt	(BF29G)
	6BA Threaded Spacer x ½in.	1 Pkt	(LR72P)
	6BA Brass Studding	1	(FW15R)
	1mm Vero Pins	1 Pkt	(FL24B)
	Diecast Box	1	(LH72P)
	Spacers Clearance 6BA x ¼	1 Pkt	(FW34M)
	Spacers Clearance 6BA x ½	1 Pkt	(FW35Q)
	Heatshrink Sleeving CP95	1 Mtre	(YR17T)
	Heatshrink Sleeving CP24	1 Mtre	(BF87U)
	Kit (P) PLAS	1	(WR23A)

OPTIONAL

Min Mains White. 3 core	As req	(XR02C)
Twin Mains DS White	As req	(XR00A)
Zip Wire Twin	As req	(XR39N)
Potting Compound	1 Pkt	(FT17T)
240V 60W Domestic Light Bulb	1	
Lamp Holder. Inspection Type	1	

A complete kit of parts is available, for this project, but does not include optional items:
Order As LK94C (Hobbyists Temperature Controller Kit) Price £24.95
The following items are also available separately, but are not shown in our 1986 catalogue:
Hobbyists Temperature Controller PCB **Order As GD00A Price £2.80**
High Volts PCB **Order As GD01B Price £2.70**
Temperature Controller Front Panel **Order As FA85G Price £1.80**

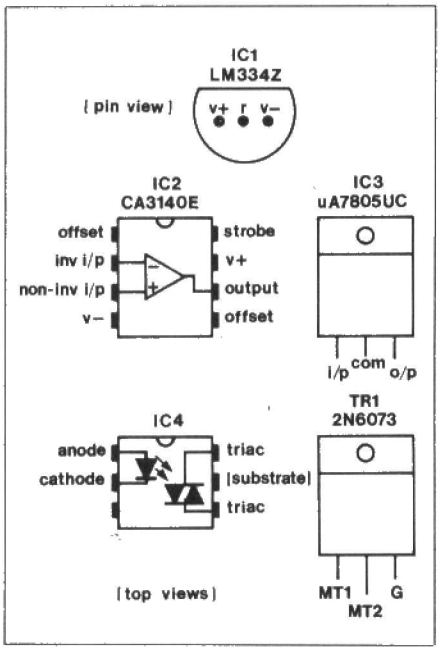


Figure 6. Pinouts

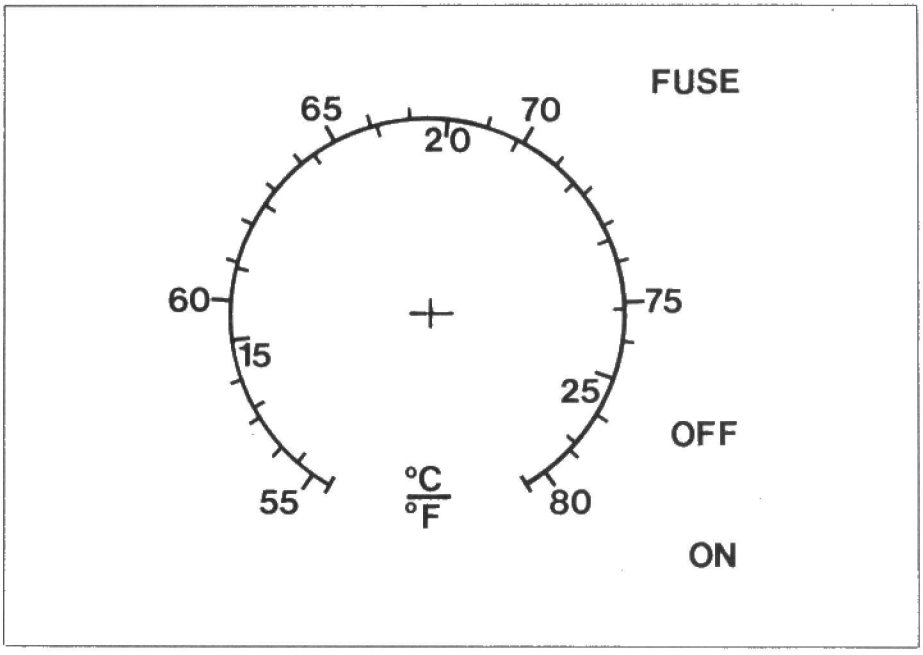


Figure 7. Temperature Scale

and low voltage wiring. If no mica mounting set is used on the power triac TR1, don't forget that the securing bolt through the insulating board will be live with mains potential. High voltage connections should be covered with insulating sleeving.

The boards and other components may then be mounted on the inside of the box lid taking care to arrange adequate clearance between the heatsink vanes and the bottom of the box (Fig. 9). The heatsink vanes can be bent if necessary and a sheet of plain matrix or plain fibre-glass board glued inside the box is an added precaution.

Holes should be provided in the box (Fig. 10) for sensor, mains and heater leads, the cables being clamped to avoid strain on the connections. Slots should be cut in the box sides and covered with a grill to provide ventilation for the internal power triac heatsink. A further small hole is needed in the side of the box to allow for adjustment of the temperature calibration preset RV1.

The probe itself (Figure 11) should be constructed in a suitable piece of insulating tube (e.g. an old pen, test-tube) and sealed, preferably with a potting

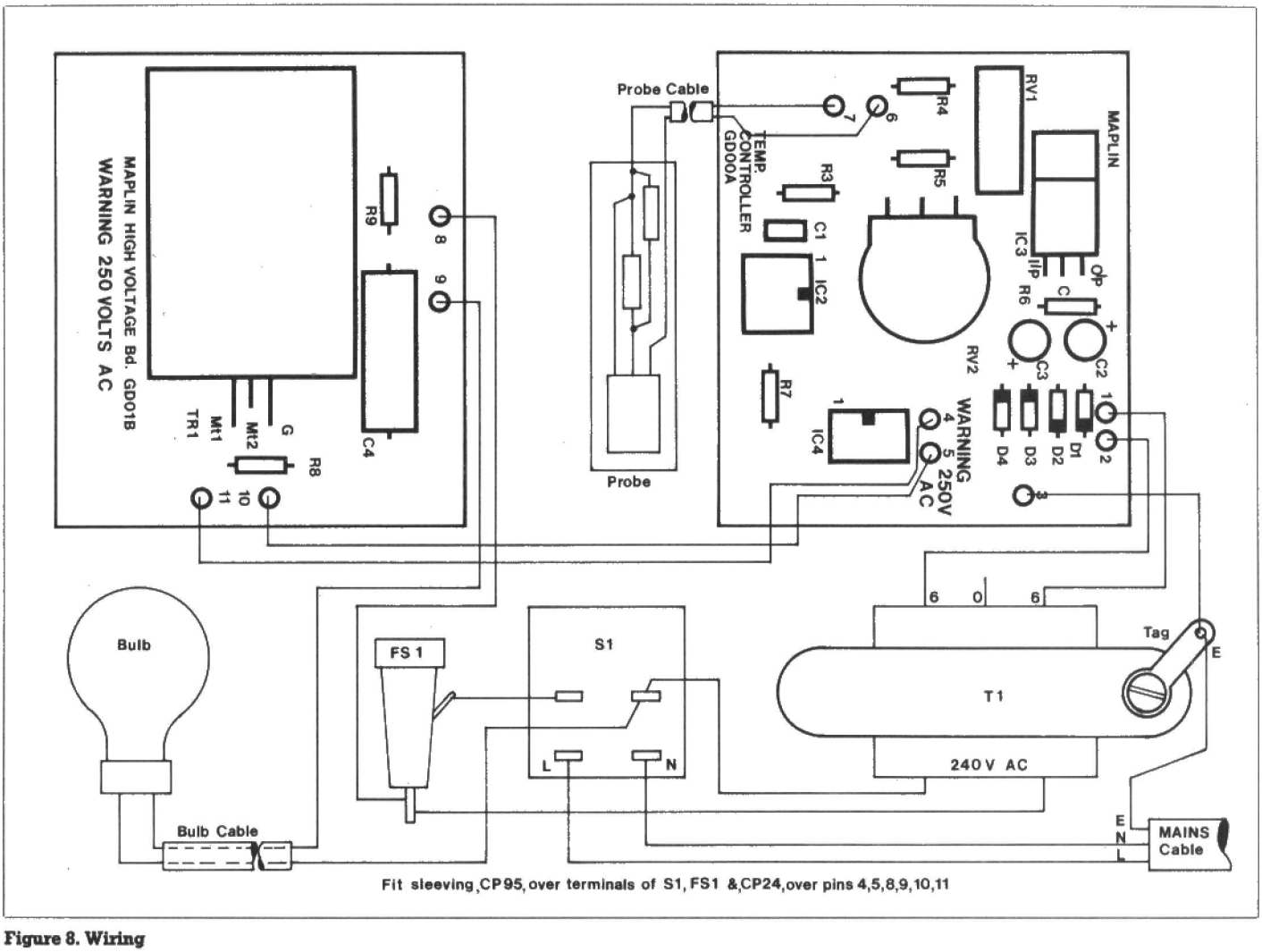


Figure 8. Wiring

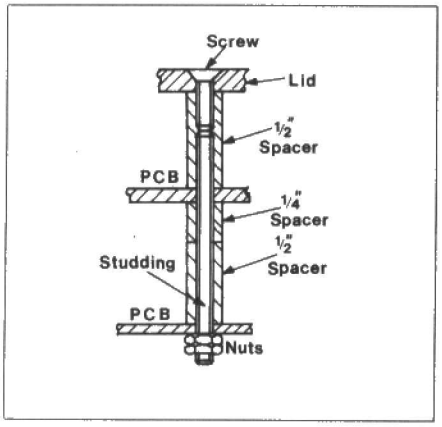


Figure 9. PCB Mounting

compound or Araldite. This not only provides strength and prevents ingress of moisture, especially when the probe is immersed in water, but also provides a certain amount of 'thermal inertia' to prevent the switch action from 'chattering' when close to the set temperature.

Now the wiring should be checked with special attention to all parts of the mains circuit. The box is closed up making sure that the circuit boards are correctly orientated with preset RV1 aligned with the adjustment hole in the case.

With applications using a mains light bulb for heating, adequate protection against accidental blows should be provided using a ventilated box or cage arrangement.

Setting Up

The unit should now be calibrated. Find a suitable temperature stable room e.g. an airing cupboard, of which the temperature is in the range covered by the unit. Set the knob of RV2 to the surrounding temperature as measured with a thermometer. Connect up the unit and turn on. Take an insulated adjustment tool and vary preset RV1 until the heater/lamp just switches. The unit is now aligned and ready for use.

Applications

For the originally intended application to home brewing, the most convenient set up consists of a cabinet of some kind in which sufficient fermentation vessels can be placed to meet requirements. In most brewing work, a steady temperature in the range 15–25°C (or 60–75°F) is preferred. The cabinet itself can take many forms but the author prefers a chest arrangement which is inobtrusive in the spare bedroom where it usually resides. Double walled construction with fireproof insulation between, seems to work well. The control unit should be fixed outside of the heated chamber/area for access and adequate cooling of the electronics. The sensor should be fixed to the inside of the cabinet, not too near the top or near the heater lamp; otherwise false readings could result.

A very similar arrangement is useful in a greenhouse propogator where temperatures around 20°C (68°F) are needed to give an early start to plants in

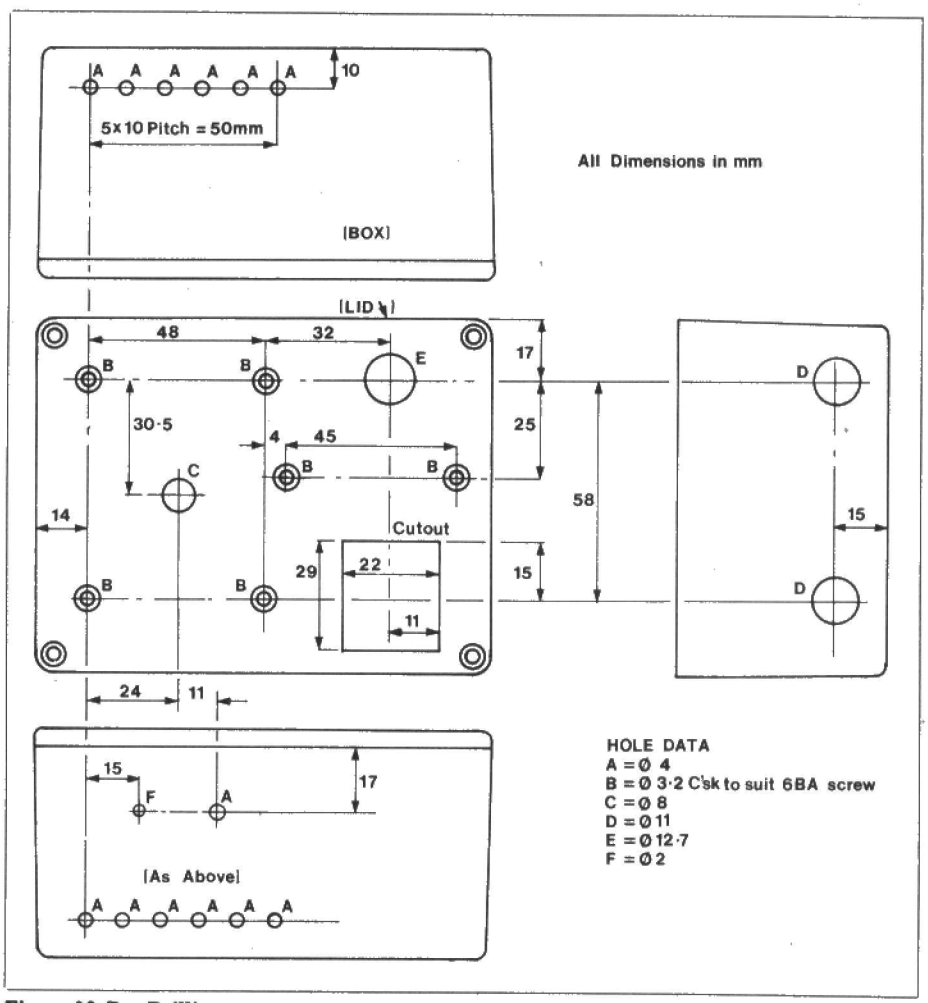


Figure 10. Box Drilling

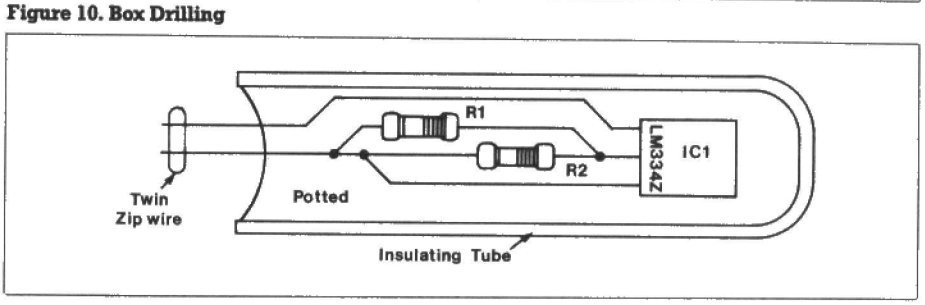


Figure 11. The Probe

spring and to maintain the more exotic hot house plants through the winter. For this application, particular care must be taken to make the mains heater waterproof as there will be a lot of water and condensation about. A sealed bulkhead lampholder is suitable here. Also, careful placing of the control box is needed e.g. mounted on a nearby wall, to avoid accidental splashing.

The unit can also be used for heating liquids. For tropical fish aquaria, the heater bulb is replaced by a proper aquarium heater made for the purpose. The heater turn-on surge current should not exceed 4 amps when using the power triac recommended. Temperatures around 23°C (75°F) are usual for this application, slightly lower temperatures being tolerated by the hardier types e.g. Angelfish, while some other types may prefer the temperature adjusted a little higher e.g. the Labyrinth Fish. To be able to adjust the temperature easily will be especially appreciated by those intending to breed tropical fish, convenient adjustment not being possible with the cheaper fixed temperature thermostats commonly used.

The same arrangement is also well suited to photographic processing requirements. For this, all the chemicals needed for a particular operation may be equilibrated to the same temperature of choice by standing their bottles in a bowl or water bath (called a 'tempering box') in which the aquarium heater and temperature sensor are immersed.

If for any application the temperature range is inadequate, it may be altered by changing the values of R4 and R5. Adding so much to one resistor and subtracting the same amount from the other will bodily shift the temperature range covered while keeping the span of degrees covered by the control RV2 the same. The scale, as shown in Figure 7 will, of course, have to be redrawn.

More powerful heaters can be used if the heater bulb is replaced by a mains relay, which opens up such possibilities as central heating control. Whatever the application the required temperature is set by one simple dial adjustment.

by Dave Goodman

FOR LESS THAN £70

ASCII ENCODED KEYBOARD

- ★ Full ASCII Set Inclusive of Upper/Lower Case Alpha, 31 control CHR$, 21 Shift CHR$ and Special Functions
- ★ 8-Bit Plus or Minus Strobe O/P data bus, TTL compatible
- ★ Any Key Down Output
- ★ Data Ready with delay and repeat output
- ★ Will fit directly to the Maplin High Quality Alphanumeric Keyboard

The keyboard electronics have been incorporated onto a large circuit board which will accommodate our 61-key keyboard (YJ12N) without number pad. All key scanning, debounce, rollover and encoding circuitry are kept to a minimum by using the General Instrument KB3600 mask programmed processor. Standard ASCII seven bit codes are produced with bit 8 available from a non-latching, dedicated key.

Externally connected systems such as micro computers, processor modules or RS232 encoders can be reset from the keyboard and connections to the module are made via a 20-way IDC, flat ribbon wire, connector. The data bus output is TRI-STATE for direct connection to processor buses and data can be strobed by either a logic high or logic low output enable signal. As any key is pressed, an active low output ($\overline{AKO}$) signals this fact and when generated codes are stable on the bus, a 52μs active low pulse is presented on the $\overline{RDY}$ output line. If a key remains held down, the $\overline{RDY}$ line, after 0.5 seconds, repeats the pulse at approximately 100ms intervals with pulse width remaining constant at 52μs during this period until the key is released. Both of these outputs are open collector for TTL interfacing, but will require pull up resistors for HC or CMOS use. System clock and clock divide by 4 outputs are brought out for synchronising purposes if required and a reset output can be generated from the keyboard.

Circuit Description

The processor IC1 handles all necessary scanning and debouncing of each key connected on the matrix in Figure 1. When a key closure is detected, the debounce routine is executed and if the key is still depressed after this routine period, then the seven bit code, for this key, is transferred to the data output bus pins and IC2. A data ready strobe is activated which is a pulse from IC1 pin 16 and a voltage level from pin 13. The scanning process is then started over again.

If another key closure is detected at some other co-ordinate, the entire sequence is repeated to encode this new key. As key closure could be detected for an already encoded key; in this case it is ignored and the code of the last key encoded remains latched on the data lines until the next code is strobed out. Single key closures, lasting for half a second or more, produce a repeated pulse on the $\overline{RDY}$ output at approximately 100ms intervals or 10Hz. The auto-strobing terminates immediately upon release of the key or upon the closure of another key. In the latter case, the codes for all depressed keys output singly without the auto-repeat feature. Table 1 lists ASCII codes and symbols where normal (unshifted) alpha codes are for lower case. Upper case values are produced with either of the two SHIFT keys. Control code values (0-31) are produced by using the CONTROL key and all code values are in the range 0-127 decimal on D0-D6. Bit eight (D7) can be generated via the BLANK (unmarked) key or during reset when all eight bits (255 D) are output. Reset is initiated by depressing the cancel key 'CAN' and carriage return key '←' together. IC2 buffers the data bus and D0-D7 outputs are tri-state, i.e. high impedance or TTL levels. The bus is made active by strobing the output enable line OE and logic high or low levels can be used by inserting one of the links A or B. For logic low link A should be fitted and for logic high, fit link B. Do not insert both links

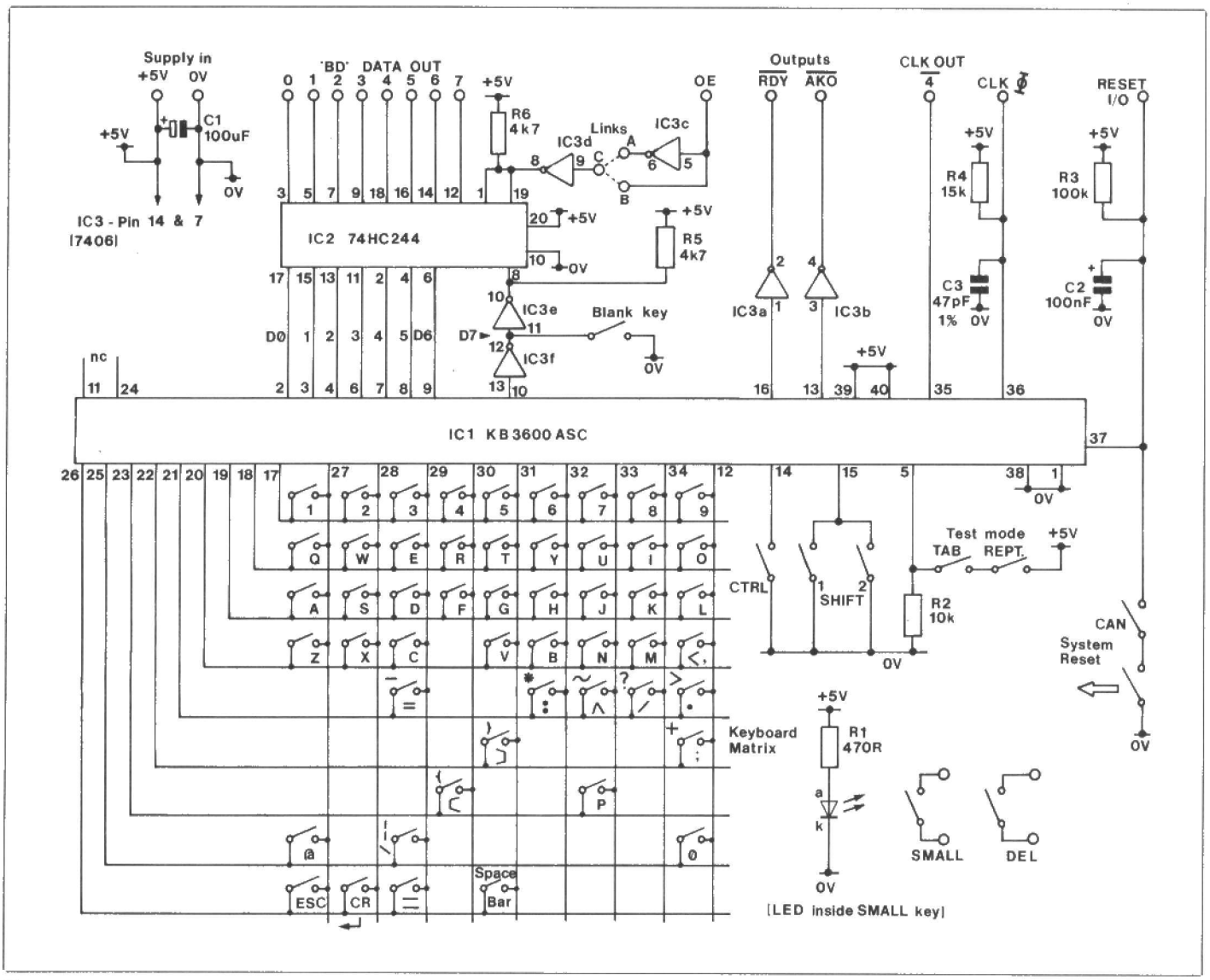


Figure 1. Circuit Diagram.

together as this may damage IC3. A power-on LED is fitted inside the SMALL key on the keyboard frame and is not shown in the parts list because of this.

Construction

Use 24-gauge tinned-copper wire to form 25 links. Each link is shown by a line on the legend between two holes, see Figure 2. Straighten a length of wire and make a right-angled bend about 5mm in from one end. Insert the formed end into a relevant hole and measure the distance required for the next right-angled bend. This procedure should be repeated for every link position, except in positions A and B.

Identify and insert resistors R1 to R6 and three capacitors C1 to C3. C3 can be fitted either way around, but C1 and C2 are polarised and the appropriate lead inserted as to the legend.

Fit the three IC sockets and SKT1. Carefully solder all component leads onto the track pads and cut off excess wire ends. Many projects fail at this point, due to poor soldering and solder splash bridges across tracks so *attention to detail is of paramount importance.* If possible, clean all soldered areas with a solvent and brush, to remove flux etc, then carefully inspect the area.

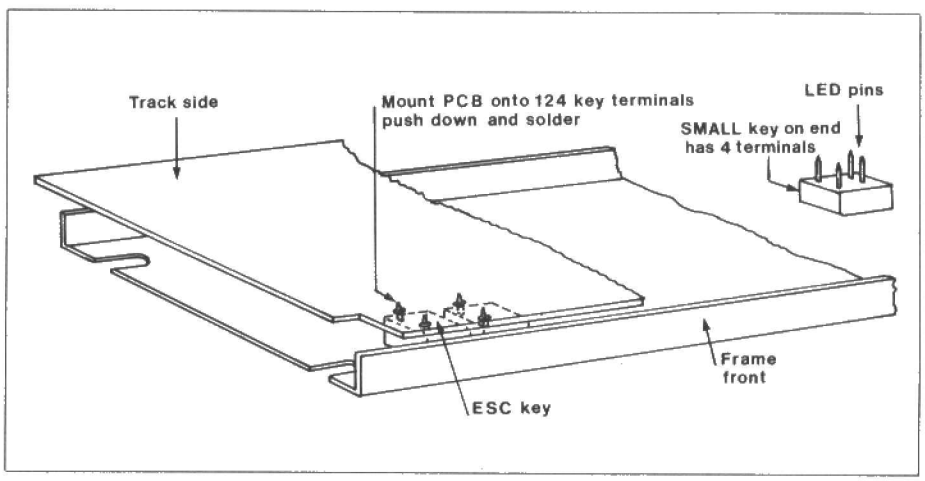
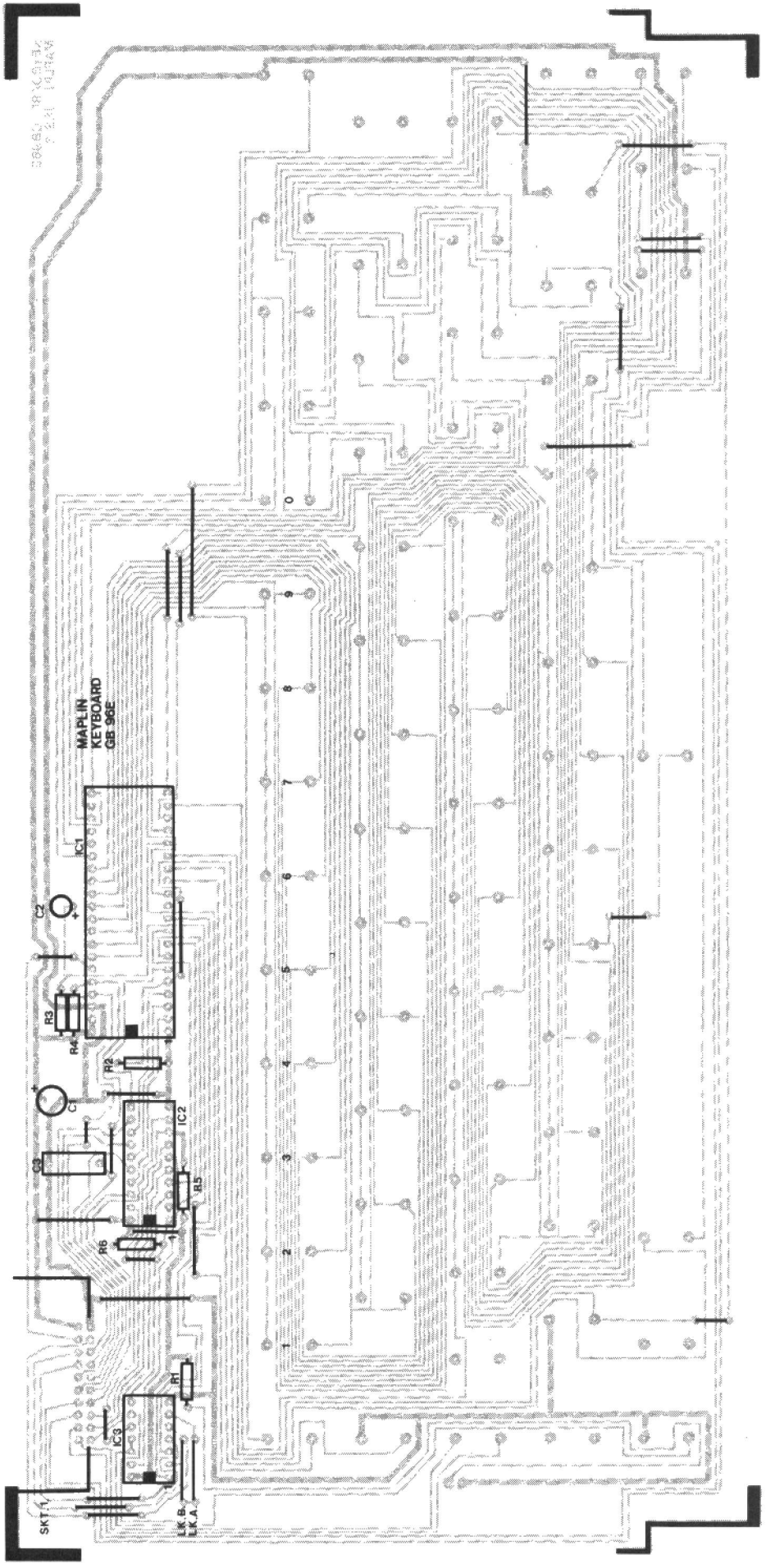


Figure 3. Mounting the PCB to the keyboard.

Keyboard

Before fitting the recommended keyboard, ensure that every key contact pin is vertical and at right angles to the key body base. If all terminals are well adjusted, then mounting the PCB is quite straightforward. The odd terminal that might be flattened in the process will cause a problem once the PCB is soldered in place! Be sure that this does not occur. Refer to Figure 3 and lay the keyboard, terminals upward, with the front space-bar nearest to you. Hold the PCB with track side upward, and electronics area facing away from you, as shown, and gently push the PCB over all 124 key terminals.

Check that all holes have a pin protruding through and solder each one. Slight pressure will need to be applied to the board while soldering to keep it flat and level. Repeat the cleaning and inspecting process and construction is then complete.



Please note that this layout is shown smaller than actual size

Figure 2. PCB layout and legend.

ASCII CHARACTER SET

CHARACTER	CODE	CONTROL	SHIFT	KEY	DEFINITION
NUL	0	@			NULL
SOH	1	a			Start Of Heading
STX	2	b			Start of TeXt
ETX	3	c			End of TeXt
EOT	4	d			End of Transmission
ENQ	5	e			ENQuiry
ACK	6	f			ACKnowledge
BEL	7	g			BELL
BS	8	h			BackSpace
HT	9	i			Horizontal Tabulation
LF	10	j			Line Feed
VT	11	k			Vertical Tabulation
FF	12	l			Form Feed
CR	13	m		↵	Carriage Return
SO	14	n			Shift Out
SI	15	o			Shift In
DLE	16	p			Data Link Escape
DC1	17	q			Device Control 1
DC2	18	r			Device Control 2
DC3	19	s			Device Control 3
DC4	20	t			Device Control 4
NAK	21	u			Negative AcKnowledge
SYN	22	v			SYNchronous idle
ETB	23	w			End of Transmission Block
CAN	24	x			CANcel
EM	25	y			End of Medium
SUB	26	z			SUBstitute
ESC	27	[		ESC	ESCape
FS	28	\			File Separator
GS	29	]			Group Separator
RS	30	^			Record Separator
US	31	—			Unit Separator
SP	32	SP	SP	SPACE BAR	SPace
!	33				Exclamation Mark
"	34				Quotation Mark
#	35				Number
$	36				Dollar
%	37				Percent
&	38				Ampersand
'	39				Apostrophe
(	40				Opening parenthesis
)	41				Closing parenthesis
★	42				Asterisk
+	43				Plus
,	44	,			Comma
–	45	–	=		Hyphen or Minus
.	46	.			Period (decimal point)
/	47	/	?		Right slant
0	48	0	0		Zero
1	49	1	!		One
2	50	2	"		Two
3	51	3	#		Three
4	52	4	$		Four
5	53	5	%		Five
6	54	6	&		Six
7	55	7	'		Seven
8	56	8	(		Eight
9	57	9	)		Nine
:	58	:	★		Colon
;	59	;	+		Semicolon
<	60				Less than
=	61				Equals
>	62				Greater than
?	63				Question Mark
@	64	NUL			

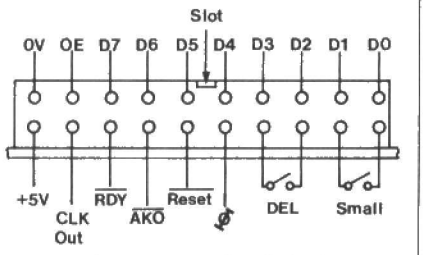
CHARACTER	CODE	CONTROL	SHIFT	KEY	DEFINITION
A	65				Upper Case A
B	66				Upper Case B
C	67				Upper Case C
D	68				Upper Case D
E	69				Upper Case E
F	70				Upper Case F
G	71				Upper Case G
H	72				Upper Case H
I	73				Upper Case I
J	74				Upper Case J
K	75				Upper Case K
L	76				Upper Case L
M	77	SHIFT	CHR$		Upper Case M
N	78				Upper Case N
O	79				Upper Case O
P	80				Upper Case P
Q	81				Upper Case Q
R	82				Upper Case R
S	83				Upper Case S
T	84				Upper Case T
U	85				Upper Case U
V	86				Upper Case V
W	87				Upper Case W
X	88				Upper Case X
Y	89				Upper Case Y
Z	90				Upper Case Z
[	91	ESC	{		Opening Bracket
\	92	FS			Left Slant
]	93	GS	}		Closing Bracket
^	94	RS	~		Circumflex
—	95	US	delete		Underscore
`	96				Grave Accent
a	97	SOH	A		Lower Case a
b	98	STX	B		Lower Case b
c	99	ETX	C		Lower Case c
d	100	EOT	D		Lower Case d
e	101	ENQ	E		Lower Case e
f	102	ACK	F		Lower Case f
g	103	BEL	G		Lower Case g
h	104	BS	H		Lower Case h
i	105	HT	I		Lower Case i
j	106	LF	J		Lower Case j
k	107	VT	K		Lower Case k
l	108	FF	L		Lower Case l
m	109	CR	M		Lower Case m
n	110	SO	N		Lower Case n
o	111	SI	O		Lower Case o
p	112	DLE	P		Lower Case p
q	113	DC1	Q		Lower Case q
r	114	DC2	R		Lower Case r
s	115	DC3	S		Lower Case s
t	116	DC4	T		Lower Case t
u	117	NAK	U		Lower Case u
v	118	SYN	V		Lower Case v
w	119	ETB	W		Lower Case w
x	120	CAN	X		Lower Case x
y	121	EM	Y		Lower Case y
z	122	SUB	Z		Lower Case z
{	123				Opening brace
¦	124				Vertical line
}	125				Closing brace
~	126				Tilde
—	127				Delete
MODE	128	SPECIAL		BLANK	Add to CHR – non latching
TEST	240	FUNCTION		TAB REPT	Add to CHR – non latching
RESET	255	KEYS		CAN←	

Table 1

Using the Keyboard

Figure 4 shows socket connections which can be made using a 20-way IDC plug and cable (see Parts List). An external 5V @ 85mA power supply is required for the electronics which should be well regulated. Two keys 'DEL' and 'SMALL' which are single pole, make action types are not used, but are available from SKT1.

The voltage and current rating of the contacts are low and must be kept to TTL or low power levels – do not connect to mains! (These contacts are non-latching.) As a general example, the D0-7 bus could be connected to a Z80A or suitable processor bus and either RDY or AKO connected to an interrupt input bus. When a key is depressed, the processor interrupt routine should be designed to output enable the keyboard bus and read the available data. Any connections made between keyboard and processor systems should be kept short so as to



Rear view of keyboard showing 20 way IDC socket

0V, 5V	Power supply 5VDC @ 85mA input.
$D_0 - D_7$	Tri-state 8-bit data bus output (TTL levels)
OE	Data bus output enable, for logic high or low signals.
Ø	System clock output, ≃ 950kHz.
CLK OUT	System clock ÷4 output, ≃ 238kHz.
$\overline{\text{RESET}}$	Turn on reset input, or keyed reset output.
$\overline{\text{RDY}}$	Active low, data ready strobe O/P with repeat.
$\overline{\text{AKO}}$	Active low, any key down output.
DEL	Spare 'DEL' key contact output.
SMALL	Spare 'SMALL' key contact output.

Figure 4. Output socket connections.

avoid unwanted RF transmission and noise pick up, otherwise problems will be encountered. Timing waveforms are shown in Figure 5.

The industry standard UART 6402 or AY-3-1015 could be configured for serial data transmission quite easily, and along with the Maplin (LK17T) TTL to RS232 level converter – and suitable power supply voltages – an RS232 ASCII keyboard can be made.

Keyboard Case

A stamped metal case is available to house the keyboard, and Figure 6 shows assembly of the unit. If the 20-way SKT1 has locking lugs fitted, then these will have to be removed to allow the lid back panel to be fitted. The socket can be accessed through a slot cut in this panel by the constructor.

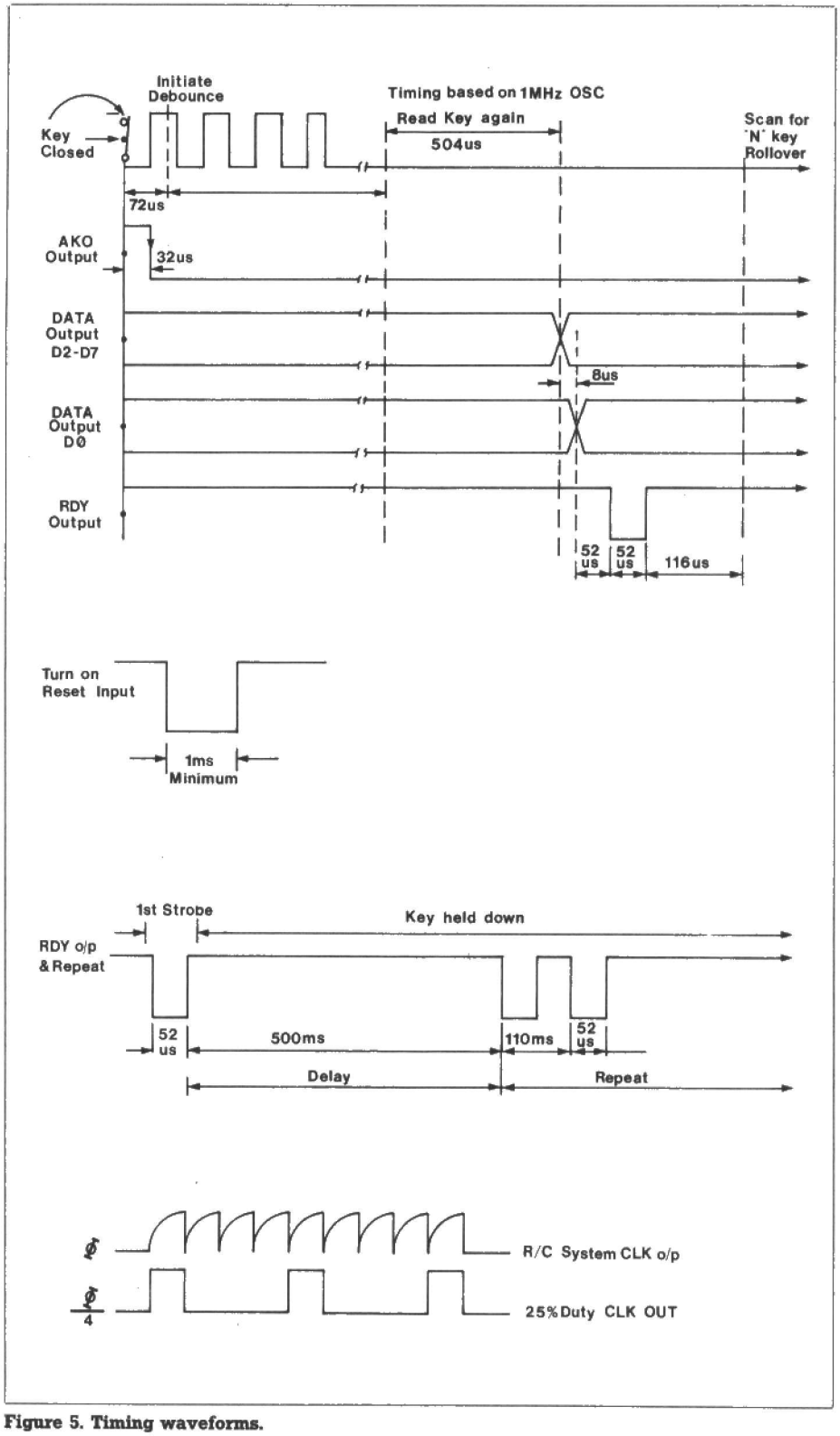
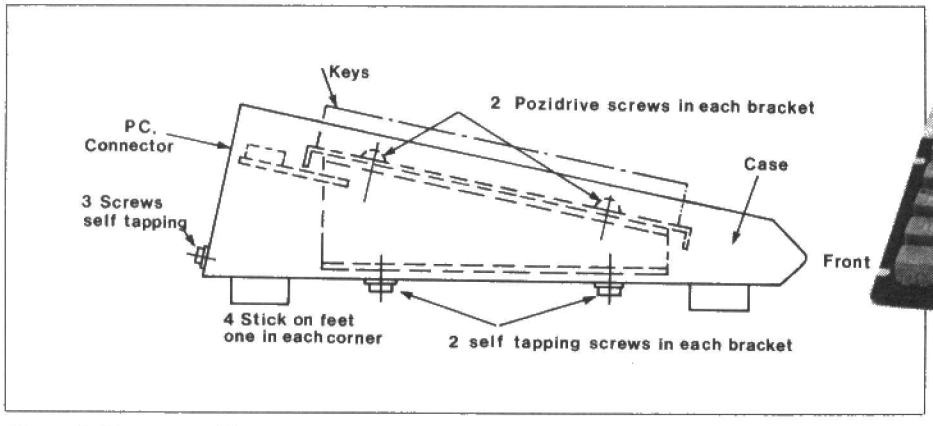


Figure 5. Timing waveforms.



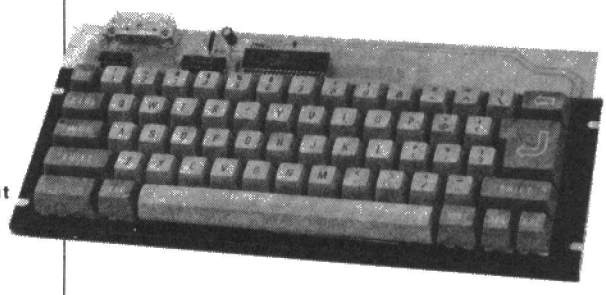


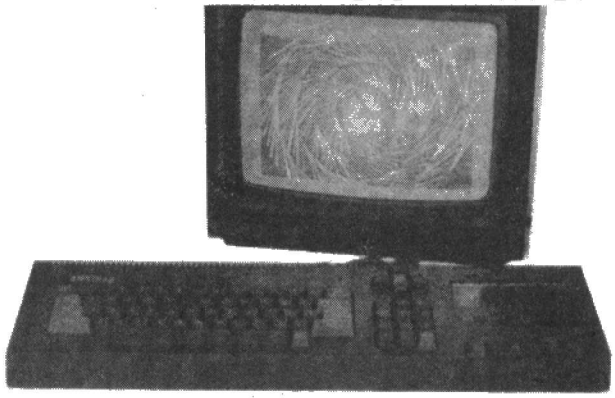
Figure 6. Case assembly.

ASCII KEYBOARD PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1	470R	1	(M470R)
R2	10k	1	(M10K)
R3	100k	1	(M100K)
R4	15k	1	(M15K)
R5,6	4k7	2	(M4K7)
CAPACITORS			
C1	100μF 10V P.C. Electrolytic	1	(FF10L)
C2	100nF 35V Tantalum	1	(WW54J)
C3	47pF Mica	1	(WX09K)
SEMICONDUCTORS			
IC1	KB3600 ASC	1	(RA60Q)
IC2	74HC244	1	(UB65V)
IC3	7406	1	(QX75S)
MISCELLANEOUS			
	Keyboard PCB	1	(GB96E)
SKT1	PCB Header Conn. R/A 20-Way	1	(FT72P)
	Strapping Wire	1 Roll	(BL14Q)
	DIL Socket 14-Pin	1	(BL18U)
	DIL Socket 20-Pin	1	(HQ77J)
	DIL Socket 40-Pin	1	(HQ38R)
OPTIONAL			
	Keyboard Mechanism	1	(YJ12N)
	Keyboard Case	1	(YJ15R)
	20-Way IDC Skt & Cable	1	(FJ02C)

A kit of parts, excluding optional items, is available for this project:
Order As LK78K (ASCII Keyboard Kit) Price £19.95
The following item included in the above kit list is also available separately, but is not shown in the 1986 catalogue:
ASCII Keyboard PCB **Order As GB96E Price £8.50**

AMSTRAD EXPANSION NEWS!!!



We are currently developing a range of projects for the Amstrad CPC 464, 664 and 6128 computers, to expand the capabilities of these excellent machines.

The first project, soon to be available, is an expansion ROM and BUFFER/DECODER which takes up to 8 ROMs, each switch selectable for 2, 4, 8 and 16K types. Most of the commercially available ROMs can be fitted.

The DD1 disk drive can also be accomodated on the CPC 464.

To follow there will be a 'Mother Board' with 6/12 Euro-card sockets for use with INPUT/OUTPUT ports, Video Digitiser, EPROM Programmer, RS232 and PSU, all of these cards will become available in the near future. For further details of these projects please write (not 'phone) the Sales Manager, P.O. Box 3, Rayleigh, Essex, SS6 8LR, enclosing S.A.E. (9 x 4 inches approx.).

MAPLIN SERVICE

With most electronic projects, performance will depend on the conditions of use. Recommendations and suggestions made in the articles in this magazine are for guidance only, since conditions of use are beyond our control.

Repairs and Get-You-Working Service

Our 'Get-You-Working Service' is available for any of the projects published in this magazine, *provided* they are constructed on our ready-etched printed circuit boards, and that they use a majority of components supplied by us. We regret we *cannot* extend this service to the 'interest' circuits, for which we do not provide ready-made boards, or supply as projects or kits; nor for projects or kits that have been *customised or modified by the constructor.*

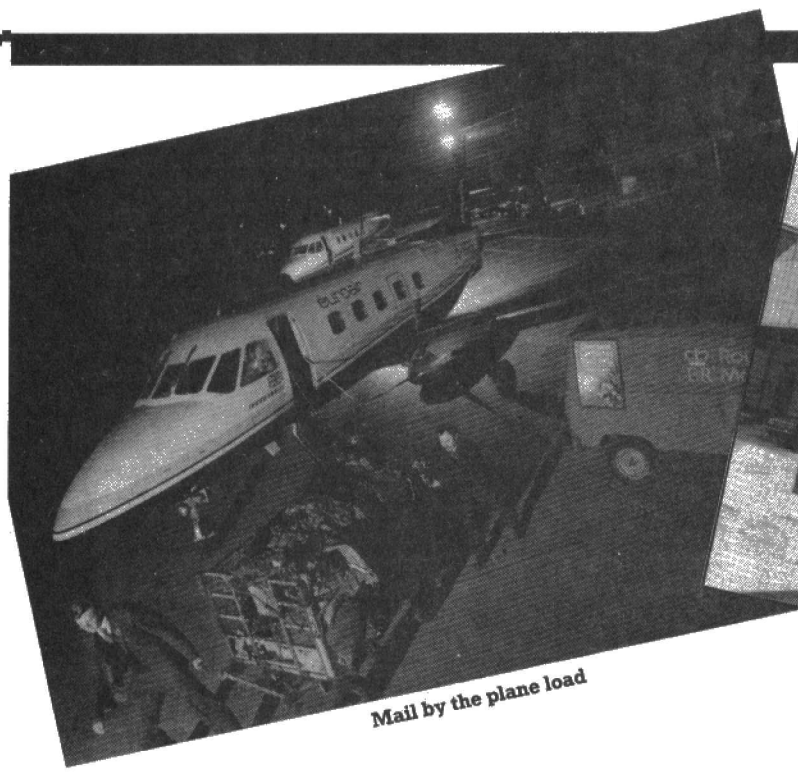
We cannot enter into correspondence with regards to fault-finding, and recommend you return the unit to us for servicing if you are unable to rectify the fault yourself.

Project Servicing

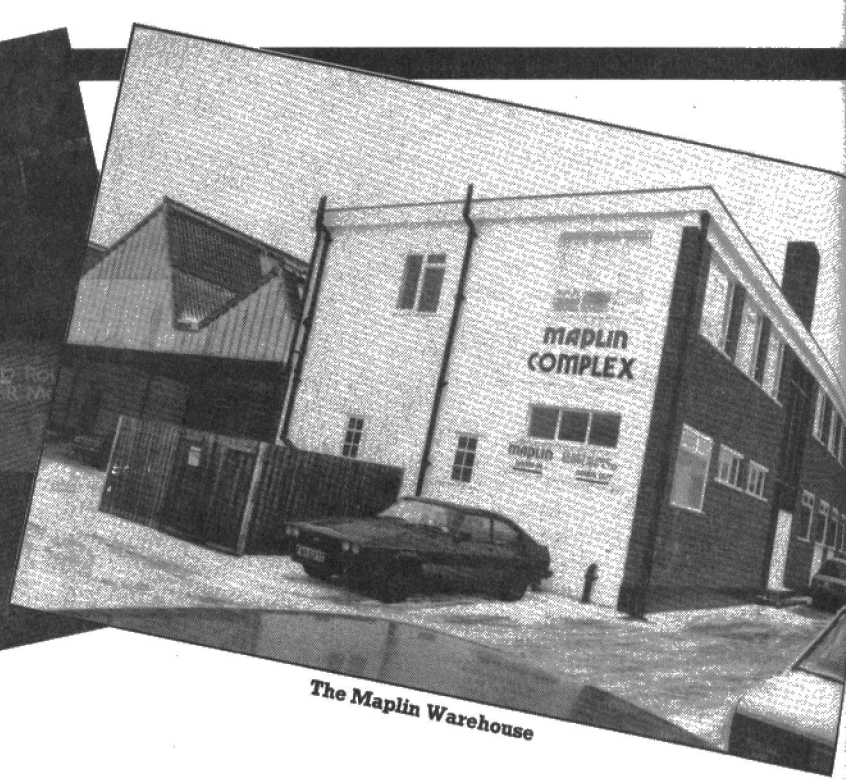
If the problem has been caused by a faulty component supplied by us, then there will be no charge for the work performed or the components used. If the fault has been caused by error(s) in construction, then there will be a charge for the work performed at a rate of £10 per hour, or part of an hour plus the cost of any damaged components which need to be replaced. If *no fault* is found on the unit, then there will still be a charge of £10 per hour or part of an hour *for the time involved in establishing this fact.*

Projects returned for repair should be addressed to:–

Service Department
Maplin Electronic Supplies Ltd
P.O. Box 3
Rayleigh
Essex
SS6 8LR



Mail by the plane load



The Maplin Warehouse

MAKE IT WITH MAPLIN

by David Snoad
Part Four

The Maplin story concludes this issue with a look into the Head Office/ Warehouse, the home of the mail order division. Without giving away any trade secrets or providing the Maplin rivals with the opportunity for industrial espionage within the pages of 'Electronics', I will attempt, in brief, to explain how Maplin have grown to be the largest and most respected electronic component retailer in the U.K.

Industrial Relations

One of the largest singular reasons for Maplin's steady growth, has to be the dedication shown by the directors and employees alike. In contrast to many contemporary firms, at Maplin there is a freedom for expression, created in an atmosphere where self motivation is seen as far more rewarding than the big stick. Good industrial relations are taken for granted, with the majority of staff having been with the company for many years.

Speaking from experience, after nearly eleven years with Maplin, it has been interesting for me to be part of the team involved with testing new ideas and ways of developing the business.

The most innovative idea for improving communication along with staff involvement and awareness, must be the Monday morning Bingo sessions. The what!!! I hear you say, yes, every Monday morning at 9.00 am sharp, the Managing director addresses all the employees located at the head office and advises them of the previous weeks performance. This is also an opportunity to provide information on any events involving the company or any new ideas or changes in procedure. The announcements are followed by a couple of games of Bingo, where the prize values are dependant on the amount of orders received the preceeding week – and the prize is doubled if all the orders have been dealt with. The bingo livens everyones spirits and almost makes getting up on a Monday morning seem respectable.

The Day Begins

After Bingo comes the serious task of handling the days business. The first batch of mail is opened early by the girls in what's called the Front Office. Later deliveries from the post office box are handled as the day progresses. It is rewarding on occasions to explain to amazed customers how it is possible for them to post an order one day and receive their goods by return post the following morning. This is possible because, post permitting, mail which is posted by customers first thing in the day can occasionally reach our post box before the late collection. These orders can then sometimes be input into the computer, collected and packed before the final post leaves at 4.30 pm.

Working Environment

Naturally, the smooth progress of an order through the system relies on several departments working together as a single unit. A major contribution to this joint co-operaton is the recognition by directors and staff that every function has its own importance, no single department is considered to be more valuable than

The 'Front Office.'

any other. On the one hand, the accounts and credit control departments to, on the other, the kits section where several staff are employed compiling all the items necessary to generate the extensive range of project kits which Maplin now supply. A close harmony exists between departments and employees, which creates a working environment which many large industries would do well to watch. A combination of the friendly family business on the inside and yet, on the outside the strength of a growing corporate image, an image which is supported by the ever expanding Maplin catalogue.

The Warehouse

Maplin have now occupied the same warehouse for about 7 years, moving in during the winter of 1978. When we first saw the empty 15,000 sq.ft. shell, we considered that a decade would pass before we would ever need so much space, but that theory was soon to be proved wrong. Within a couple of years, mezzanine floors were being constructed and it seemed inevitable that another move would be necessary. It was around this time that fate showed a helping hand, rumours were confirmed that the two adjoining warehouse units would become vacant in the near future.

The near future drifted on rather more than everyone would have liked, but by the end of 1983 Maplin acquired two further factory units with offices which doubled the amount of space available to 30,000 sq.ft. There was an immense amount of work to do converting one of the factory units from what used to be a dairy into a new open plan office, this was completed by the spring of this year to the satisfaction of all the office staff, who now not only enjoy but appreciate their new surroundings.

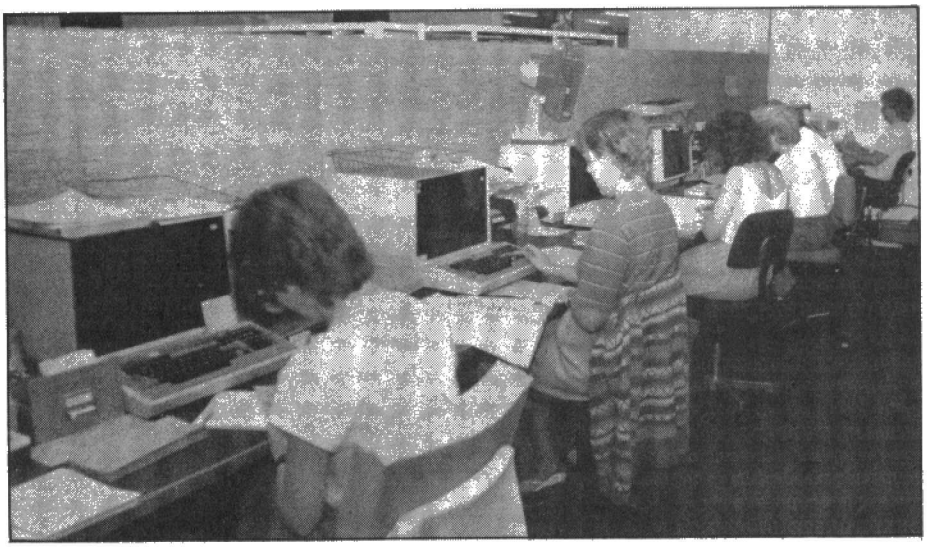
Goods In – Post Out

After enlarging the offices, the rest of the factory space was used for expanding the stores area. Part of the new building contained a loading bay which was quickly designated the 'goods in' area. This provided an ideal situation where stores staff could off-load and unpack our incoming stock, on average between 500 and 1000 parcels per week – the products can then filter through the building, become part of a customers order and then pass on to the post and packing department at the other end of the building. The Post Room staff have their own loading bay and keep the Post Office happy to the tune of about 5000 packages per week. Being the largest postal user in South East Essex, Maplin co-operate closely with the Post Office and are able to benefit from the excellent delivery/collection service which the Post Office provide.

Order Entry

After the mail has been opened it is passed to the Order Entry or invoice department and, as can be seen by the

Another mail-van leaves loaded with customers' goods

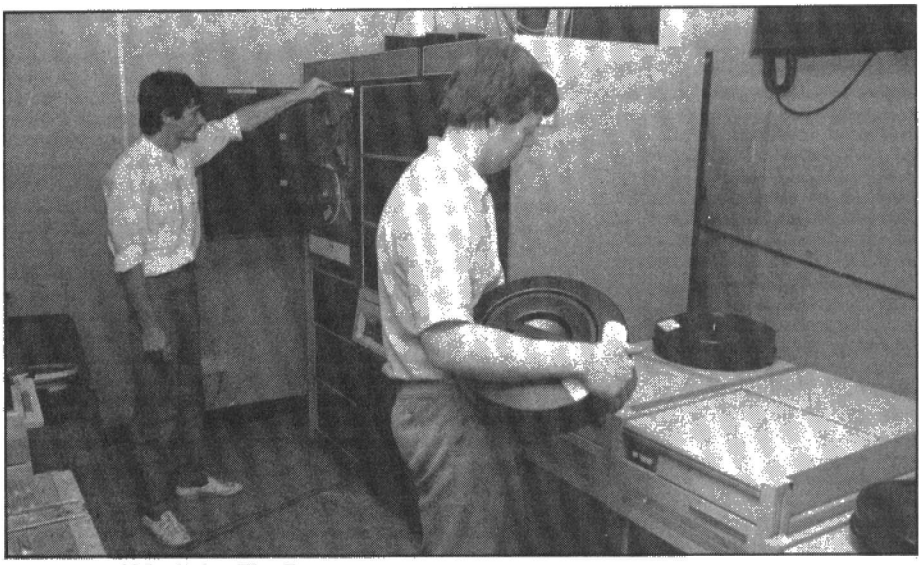


Order Entry

picture, the order entry procedure is completely computerised as are nearly all the important administrative tasks within the company. The invoice department has 7 of the 48 terminals which are dotted around the building. Trained operators then process the orders by calling up each customer from the computer, using the customer number when provided, then all the necessary information is added to the customer file which provides a fast, efficient way of recalling any customer details should it be necessary.

The Computer

The Maplin operation is controlled by a PDP 11/70 computer, and any interested buffs might like to know that we use the RSTS/E operating system. The Data Processing Manager, Nigel Fawcett, programs the computer with his assistant, they mainly use BASIC and sometimes Macro 11. Not unaturally many people believe that the BASIC language is one that was developed as a domestic fun language but, of course, it is used extensively throughout commerce and industry as well. Nigel, who is now



The Heart of Maplin's – The Computer.

married with 2 children, has been with Maplin for 9 years, starting as a salesman at the Westcliff shop. After about two-and-a-half years he was transferred to the Head Office where he looked after the telephone sales office. A year later during the winter of 1979 the first computer was installed. Maplin went through a tough patch, trying to change over from manual administration to a computer system, but with inadequate support from the computer supplier. Nigel became interested while trying to help out and found he had a natural flare for programming. This helped to solve the problem, and Nigel has looked after the computer ever since. During the last few years Nigel has assisted with the development of 'Cashtel'. For the uninitiated this is a system which allows customers, with home computers and modems, to access the Maplin computer direct, one can then look through the stock files and place an order. This service has been very popular, to the extent where telephone lines are often busy. Nigel advises us that, hopefully, the service will be extened in the near future with the addition of extra lines to ease congestion.

The Collecting Area

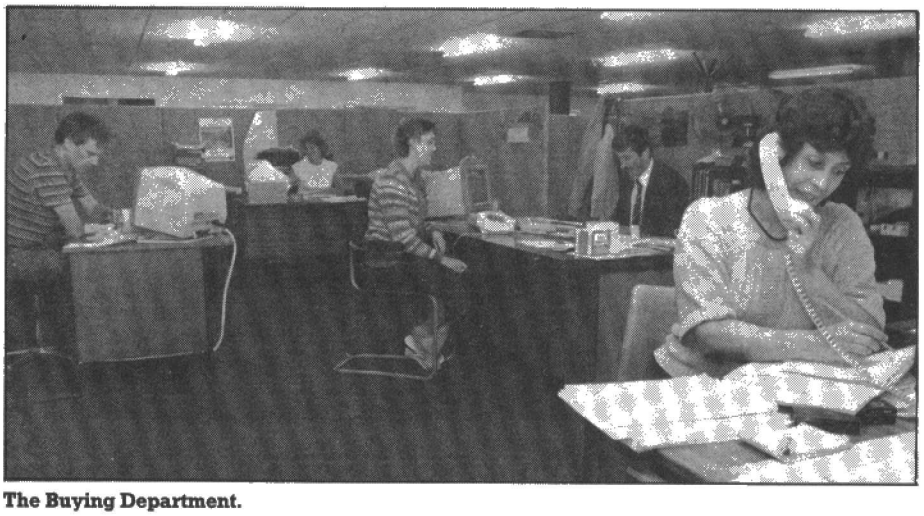
Shortly after the order has been input into the computer the Invoice/ Delivery Note is printed out in another part of the building. The collection notes are normally removed from the printer by the Supervisor Mrs. Jo Allard who organises the compiling of orders in the collecting area. The picture shows just a small corner of this large department where almost 7,000 different items are laid out.

Before printing the collection note, the computer sorts all the codes into an order which provides the collecting staff with the shortest route around the actual collecting area. Once collected the order immediately passes onto the post and packing department where it is inserted in the appropriate packaging and married up with a computer prepared address label.

Buying

Making sure that products are in the collecting area, ready for customers orders, is a buying office responsibility. The buying department is conveniently located alongside the stores and 'goods in' area. In the early years these departments were controlled by one of the directors, but for the last 8 years these duties have been managed by Mr. Lewis Bowman. Naturally the task of stock control is greatly assisted by the use of computer systems and although the computer cannot help with such important jobs as quality control, it is a very useful tool when monitoring both prices and Maplin competitiveness in the electronics retail market. As can be seen from the latest catalogue, many prices have been reduced and this is generally the result of the Maplin expansion

Orders being collected.



The Buying Department.

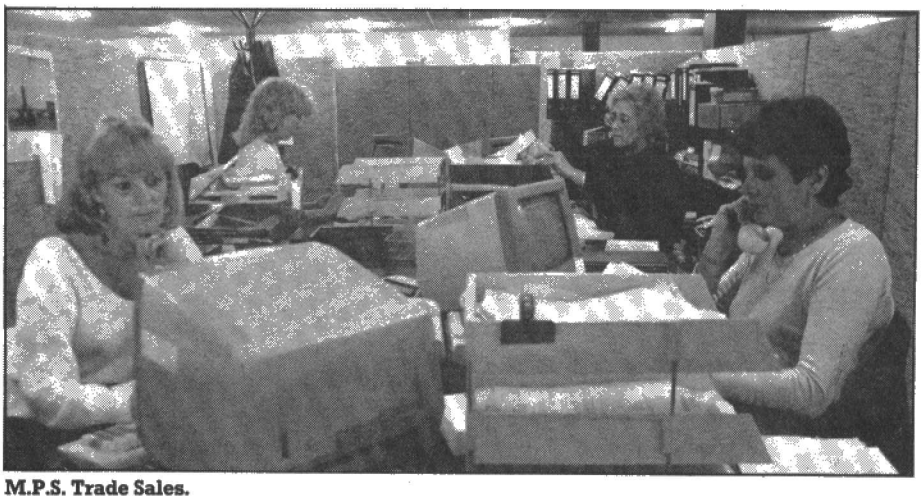
program. This gives the purchasing staff increased buying power, enables them to negotiate better deals and the benefits are passed onto the customer.

Included in many negotiations there is provision for a delivery schedule, and this helps to stabilize prices and achieve continuity of supply. Continual sourcing of new products helps to keep Maplin up-to-date with the latest technology, and regular product meetings ensure that this information is put to good use. After speaking to Lewis it is interesting to note how one facet of his job has become easier. This is simply that, because of Maplin's growth it is now rare that he has to explain who Maplin are when contacting any new suppliers!

M.P.S.

It is with the knowledge that Maplin are becoming more widely known within industrial and educational circles that prompted the emergence of M.P.S, or Maplin Professional Supplies. Maplin have offered trade accounts ever since the company started trading, but as buying power improved it became clear that Maplin could compete favourably with other wholesalers.

Not wanting retail customers to suffer as a result of trade quantity sales, it was decided to create a new post, whereby someone could control more closely the needs of trade business. Mrs. Barbara Loman was chosen, she worked from a desk within the buying depart-



M.P.S. Trade Sales.

ment where it was easy to get fast quotes and monitor the sales trends. Barbara was an ideal candidate for this post, she has now been with the company 6 years, starting in the invoice dept., and gaining further experience in the general office and purchase dept. Married with two sons, Barbara suggests that her hobby of lacemaking, which needs plenty of patience, is a pleasant contrast to the busy office and a job which she considers is the most interesting she has ever had.

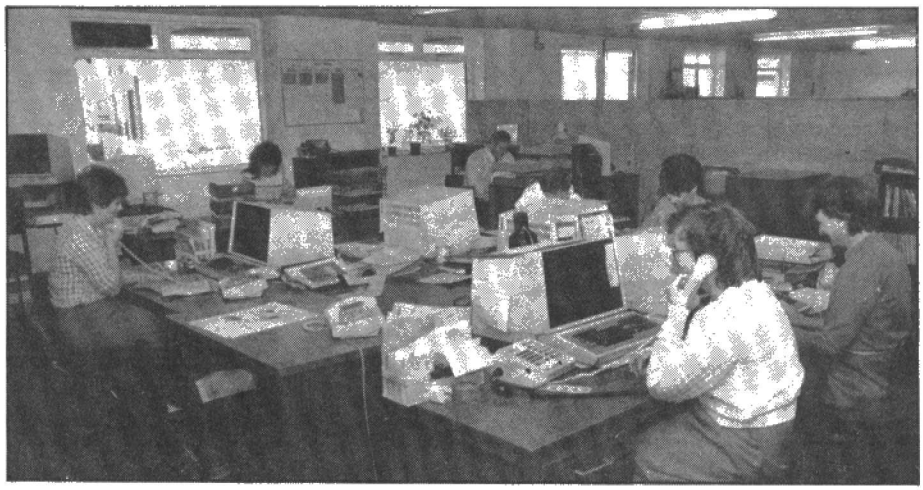
It was not long before Barbara needed assistance and this was found in the person of Carole. Starting in the order collecting area almost 3 years ago, Carole moved into the stores department and like Barbara acquired an excellent understanding of the stock code system which has proved to be a real asset.

By early this year the company had thousands of trade accounts and it was decided the time was right to set up M.P.S. This would be a trade sales division, independent of the retail sales department, but keeping the personal touch while broadening the service which is demanded by both industry and educational authorities. Barbara, as senior sales co-ordinator, looks after the department and along with Carole there is now Joanne and Lorna. Joanne, who has been with Maplin for almost a year and a half, previously gained experience in the retail sales office and Lorna who, having parents as directors of the company, had the opportunity to learn much of the system before joining as an employee. It could be said that Lorna is the longest serving employee, because she has been in and out of the warehouse since she was 4 years old. All four girls are keen to give whatever assistance they can, whether the enquiry be large or small and Barbara mentions that because of the complicated trade pricing structure, the new M.P.S. price list is only intended as a guide. Where customers require prices for larger quantities than those specified on the price list, Barbara assures us that a friendly voice awaits your call.

Retail Sales Office

Alongside Trade Sales is the Retail Sales Office, and it may be worth mentioning here that both these departments normally only handle mail order enquiries, anyone wishing to collect their goods or look before purchasing would need to contact the appropriate shop. The retail sales office is managed by John Attfield, who joined Maplin 3 years ago, starting as a computer service engineer and progressing after 18 months to his present position. Shortly before John began with the company he finished a 15 year term in the Army. Working on transport management, he has travelled all across Europe. At home John spends his time with his Wife and 2 sons when he is not fanatically involved with his computer.

The Sales Office has several functions, firstly it offers a telephone sales and enquiry service and this is handled by five staff. The senior telesales co-ordinator is Brenda who has been with Maplin for 6 years. Since joining the company Brenda has accumulated a large amount of product knowledge, over the years she has answered enquiries on everything from electronic organs to robots. The other telesales staff are June, Barbara, Ingrid and Sue. Both June and Barbara started shortly after Maplin moved to the current premises, almost 7 years ago. Looking after credit card sales, June's past experience, as an overseas telegraphist, is being put to good use. June has previously worked in the collecting area and invoicing while Barbara spent most of her first five years as the senior clerk in the post dept. With the increased use of credit cards these days, many customers are making use of the telephone ordering facility. John reminds us in this instance that the use of Maplin order codes helps to speed up the order entry and keep customer telephone costs to a minimum.



Retail Sales.

Joining the team 5 months ago, Ingrid recently moved onto the busy credit card desk. Since joining the company, Ingrid has been pleasantly surprised at how easy it is to talk to Maplin customers and she would like, along with the other girls, to thank the customers who take the trouble to write such charming letters. Re-joining the company recently after 7 years is Sue, she worked for Maplin for 2 years at the previous warehouse and it is nice to see her back. A lot has changed since Sue was last with us, for example the sophisticated computer system, it is difficult now to imagine how we would serve the Quarter Million or so customers without it! Other changes which Sue will appreciate, include the installation of a modern telephone exchange. This offers hidden advantages to the customer by saving on call costs. Previously calls were routed through an operator which meant that customers had to pay for the call while waiting for a free line to the sales department. The new exchange contains a unique queueing system for sales office telephones. Although on occasions this may mean a short delay getting an answer, it does follow that the call costs nothing until customer enquiries are actually being handled.

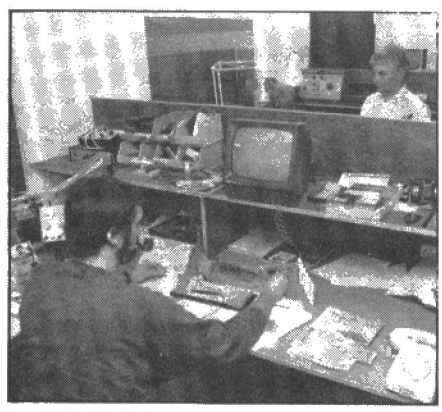
Also in the sales office is Pat who handles most of the written enquiries. Pat has been with Maplin for about 6 months and she enjoys the varied enquiries which occupy her day. Last but not least, Debbie, who occasionally assists with entering orders into the computer, but spends most of her time recording incoming parcels. This also involves looking after the administration associated with customers project servicing.

Servicing

Project maintenance is a service which Maplin offer to customers who need assistance with their project construction. Skilled technicians are available to search out those elusive clues which identify why something will not work. The trained eyes of our technical staff can often find errors quite quickly and constructors will, no doubt, be interested to know that 80% of faults are caused by incorrect soldering – often in the form of either broken tracks on PCB's, solder bridges or the ever popular dry joint.

Research and Development

Before projects can be published, they have to be designed and this task is undertaken by the Maplin Research and Development Laboratory. The chief engineer is Bob Kirsch who after 6 years with the company has been involved in many projects, too many to list here. Like the two Maplin Managing Directors, Bob



The Maplin Laboratory.

was trained on Post Office Telecommunications, maybe that is why one of his favourite projects to date is the 'Digitel' telephone exchange, although he says the 'Matinee' Organ and Train Controller were among the most satisfying to work on as well.

Bob has seen a trend in recent months towards several microprocessor related projects, but he likes to think that the lab produce an interesting variety of designs suitable for the home constructor. Away from work Bob often goes boating with his wife and two children. Boating is a strong influence in another of Bob's pastimes, this is helping to maintain the Southend lifeboat.

About once a month Bob can be found one-and-a-quarter miles from shore at the end of Southend pier, checking the radio equipment and helping to look after the engines of his favourite life saving craft. For the future, Bob will not divulge what he is working on at present, but says it is a project in which there should be a lot of interest when it is launched in the near future.

Publications Office

The main reason for developing the many electronic prototypes which materialise in our laboratory is, of course, to provide projects which can be published in 'Electronics, the Maplin Magazine'. As a reader of this journal you are no doubt aware of – and, we hope, appreciate – the difference between this and other electronic based magazines. The lack of many pages filled with repetitious advertising, means more space is available for the many feature articles, projects, Maplin news, new products and price updates.

The magazine is produced in the Publications Office. The editor is Roy Smith who has been with the company nearly 8 years. Joining as a draughtsman, Roy became a technical illustrator when the Electronics and Music Maker (E&MM) magazine was launched back in March 1981. The more ardent followers of Maplin history will remember that it was Maplin publications who first started E&MM after observing a niche for a music based electronics magazine. E&MM was soon successful but the music bias grew stronger, drifting away from the Maplin ideal. Therefore, E&MM was sold and at the end of 1981 a new magazine was launched which was 'Electronics', a house magazine to replace the newsletters which had served so well. I wonder how many readers can remember those early newsletters containing topical cartoons which started appearing in 1974. The Maplin directors can remember them well, the only area large enough to layout the large format sheets was the living room floor and it was often five o'clock in the morning when Doug, Roger and Sandra would collapse after completing yet another news sheet.

Not being involved with the newsletter, Roy must have gained experience from his hobby, as Editor of 'Monitor', otherwise known as the U.K. Atari Computer Owners Club magazine. Sounds like a busmans holiday to me.

The other publication to emerge from this office is the Maplin catalogue. This year Doug Simmons (Joint Managing Director) and his team have compiled yet another feast of electronic wizardry. Together with the Adventureland theme and new logo, Maplin have produced a different price structure which we are sure will lead us towards the 1990's with confidence.

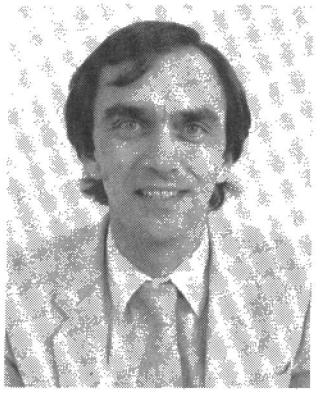
Well, we have travelled through Maplin history from past to present, now the time has come for me to thank everyone concerned for helping me to assemble this article. I hope you have enjoyed meeting some of the Maplin team and have found it interesting to see what happens when we receive a business reply envelope.

For the future, if you travel to a Maplin shop between now and Christmas, you will find a 'Software Bonanza'. To make way for new stock lines we are selling all computer software at silly give away prices. However, for all the projects you construct in the future, you'll do best if you 'Make it with Maplin'.

New Appointment

Mr. Keith Evans recently rejoined Maplin as the Manchester Store Manager. Keith has spent the past two years working for a company involved with business investments, prior to which he was Manager of Maplin's Birmingham Shop. Being involved with the setting up of the Birmingham Shop, Keith was with the company for two years before being lured away. Fortunately, for us, Keith regretted his change of job and has been pleased to accept his new role as Manager of the company's only self-service Store. Although, at first, he was rather apprehensive about self-service, Keith has been pleasantly surprised by his customers preference for the Manchester Store layout. And it did not take long for Keith to get himself involved with the proposed improvements to the Store. The changes which have been delayed, are now planned for the end of the year.

Most of Keith's early working life was spent in the RAF where he worked as an Electronics Engineer. During his 15 years in the RAF, he visited Aden, Germany and Singapore, and as if this amount of travel was not enough, when Keith finished his term in the forces, he joined the Ministry of



British Overseas Development working for the Zambia Post and Telecommunications Corporation.

Back to the present, Keith with his wife and two sons are looking forward to getting settled permanently in Manchester, and Keith is pleased to be moving to an area where he can follow one of his favourite sports, Rugby League. Along with sport, Keith's other hobbies are philately and music.

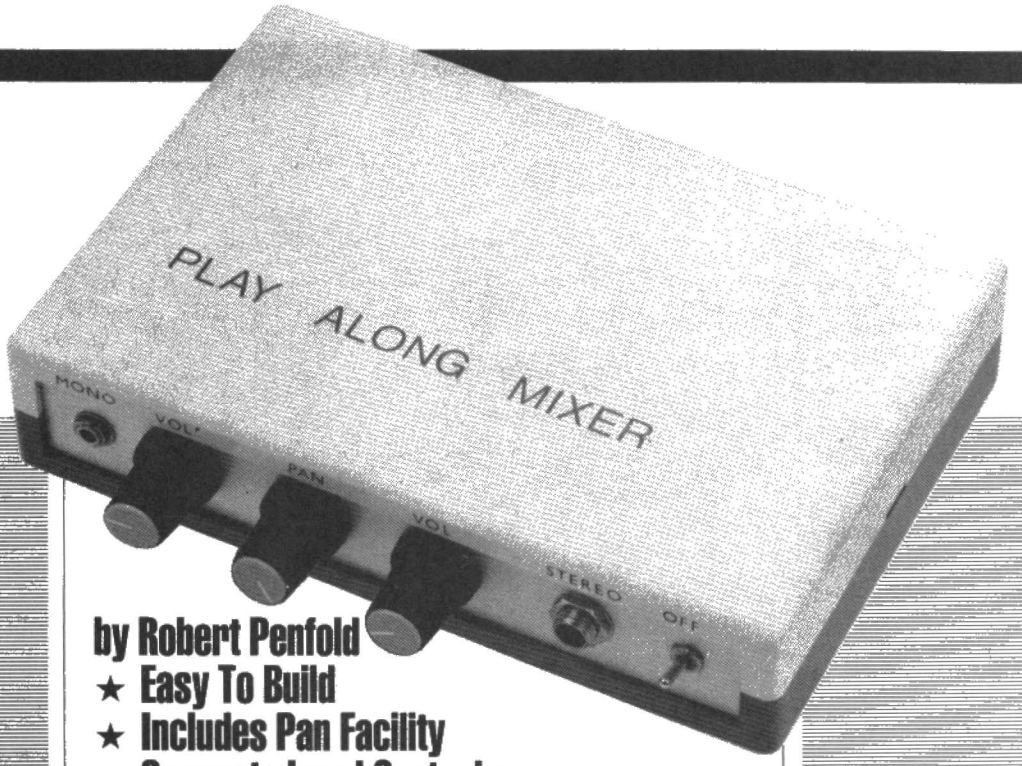
Keith has been happy to accept the challenge of his new career and, through the pages of Electronics, he would like to wish a warm welcome from his Store to all readers of this magazine.

Seen in the picture is Guy Taylor and his creation, 'Rainbow the Robot'. Guy designed his robot in response to a competition run by 'Your Computer' magazine and sponsored by Maplin who gave a Hero Jr. robot (worth £750) as a prize. The competition was developed by 'Your Computer' to test the imagination of their readers by setting them the task of designing a robot of their dreams or nightmares. There were some impressive entries but none finer than the winner, which was Guy's 'Rainbow', a robot designed to entertain and control crowds at football matches.

Guy, who said it took him two days to design and draw his winning entry, wanted to create a useful robot which he hoped could, on the one hand, help to improve attendances at football matches by entertaining the spectators with laser and water cannon shows, but at the same time, be an important tool in its use as a crowd controller by communicating messages of any disturbances and quenching tempers with the water cannon.

Maplin gave Guy a day to remember by presenting the prize at Fulham Football Club. A Rainbow look-a-like was built to amuse the press and along with Mr. Roger Allen, (Maplin's Joint Managing Director) who presented the prize, Hero Jr. spoke a few words to the reporters from Radio London and L.B.C.

The final words from Roger Allen were, "we don't envisage seeing a Rainbow on the terraces in the foreseeable future, but what a lovely idea".



by Robert Penfold

- ★ Easy To Build
- ★ Includes Pan Facility
- ★ Separate Level Controls
- ★ Play Along With Your Favourite Rockband

PLAY ALONG MIXER

An increasingly popular method of practicing one's musicianship with an electric or electronic instrument is to play along with a record, tape or whatever. This can be a very effective method of practice, as well as being great fun, and it can be achieved without the use of any special equipment. A hi-fi system can provide the programme material while a standard guitar amplifier and loudspeaker or a combo system is used to reproduce the output from the instrument. However, by processing the two signals in this totally separate way, the sound from your instrument remains rather detached from the programme material and much better results can be obtained by mixing the two signals and reproducing them through the same audio system.

The easiest way of doing this is to take the stereo output from the tape recorder or other programme source, and mix the signal from the instrument into it. The output of the mixer is then coupled to the hi-fi amplifier and reproduced through the stereo loudspeakers. With a suitable mixer it is then possible to position the instrument anywhere in the stereo sound stage. In fact, practically any mixer will suffice for this application, but most types actually provide far more inputs and other facilities than are really required and are consequently unnecessarily expensive when used in this application. They could also be relatively awkward to use. This simple mixer has been designed specifically for play along use, and it is very simple to operate. Separate level controls for the stereo signal and the instrument are provided, together with a 'pan' control which enables the position of the instrument in the stereo field to be set where desired.

System Operation

The block diagram of Figure 1 shows the basic make-up of the unit. It really just consists of two mixers, one in each stereo channel. Each mixer has two inputs, one for the stereo source and one for the instrument.

The position of a signal within the stereo image depends on its relative strength on the two stereo channels. By having the signal at exactly the same level in both channels it is placed in the centre of the stereo image. Making it slightly stronger in one channel than in the other offsets it in the sound stage to whichever side has the higher level. Although it is generally thought that a high level of stereo separation is needed in order to reproduce a wide sound field, this is not in fact true. Having a signal about 6dB stronger in one channel than in the other (about twice as strong in terms of signal voltage) is sufficient to place the signal right at one side of the sound stage. The 'pan' control therefore has to permit the level at which the mono input signal is mixed into each stereo channel to be unbalanced by a few dBs either way, in order to permit the instrument to be moved over the entire sound stage.

A level control is provided at the stereo input, and this is a dual gang type which does not permit separate adjustment of each channel, and consequently does not facilitate channel balancing. However, channel balancing will presumably be possible at the stereo amplifier or at the signal source.

Summing Mode

The mixer circuits are based on the standard operational amplifier 'summing mode' type. This uses what is little more than an ordinary inverting mode operational amplifier circuit, as can be seen from the skeleton summing mode mixer circuit of Figure 2.

Rc and Rd form a potential divider which biases the non-inverting (+) input of the operational amplifier to half the supply potential. The circuit could be powered from dual balanced supplies with the non-inverting input biased to the central earth rail, but when operational

amplifiers are used in audio applications, it is often more convenient to use a single supply rail with potential dividers to provide biasing.

If we ignore Rb for the time being, Ra and Re form a negative feedback network and the operational amplifier is in the standard inverting amplifier configuration. An operational amplifier amplifies the voltage difference across its inputs, with the output going positive if the non-inverting input is at the higher voltage, or negative if the inverting input is the one at the greater potential. The innate voltage gain of an operational amplifier (the 'open loop' gain) is extremely high at low frequencies, being typically about 100,000 times. As a result of this the input voltages only need to be unbalanced by a very small amount in order to send the output fully positive or fully negative. Here the negative feedback through Re automatically balances the input voltages. If the inverting input is too high in voltage this sends the output negative, reducing the voltage fed to the inverting input due to the coupling through Re. Similarly, if the inverting input is too low in voltage, this sends the output more positive, which in turn takes the inverting input to a higher voltage due to the coupling through Re. Under quiescent conditions the output and both inputs are therefore at half the supply voltage.

Of course, coupling an input signal to input 1 will result in the balance of the operational amplifier being upset, but the feedback action will again compensate for this. As an example, assume that Ra and Re have the same value, and that the input is taken one volt above the bias level. This increases the voltage at the inverting input, which unbalances the input potentials and sends the output negative. It will go negative by one volt, at which point the potential divider action across Ra and Re gives the original potential at the inverting input. The circuit thus acts as a unity gain amplifier which inverts the signal. This inversion is of no consequence in an audio application as inverted and non-inverted signals sound the same.

Although the gain of the amplifier is only unity with Ra and Re at the same value, it can be boosted by making Re higher in value. The output then has to change by a greater amount than the input potential in order to

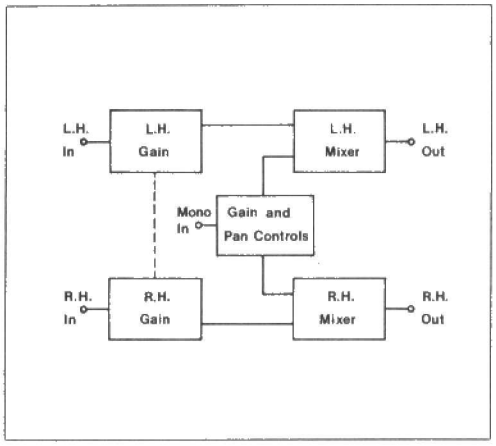


Figure 1. Block Diagram

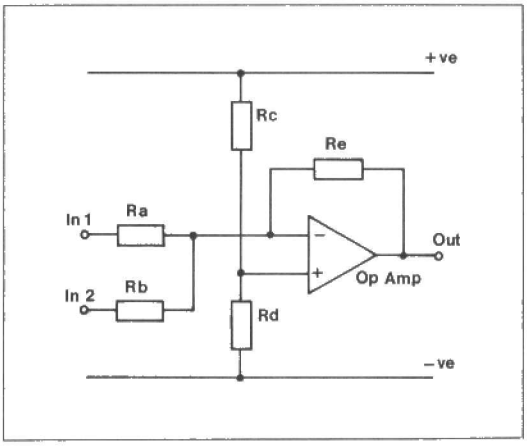


Figure 2. 'Summing Mode' Mixer

maintain the balance. The voltage gain is in fact equal to Re/Ra. Note that this is the gain of the whole circuit, or 'closed loop' gain, which should not be confused with the open loop gain.

The fundamental way in which the circuit functions is the same when Rb and input 2 are taken into account, but the output must now change by an amount that will counteract the combined input voltages. For example, if both inputs are taken positive by 1 volt, the output must go negative by two volts in order to give a current flow through Re that will counterbalance the sum of the currents through Ra and Rb, and keep the input voltages balanced. The required mixing action is thus obtained. In this application only two inputs are required, but in theory it is possible to have as many inputs as you want, simply by adding extra input resistors. Apart from signal mixing, a mixer

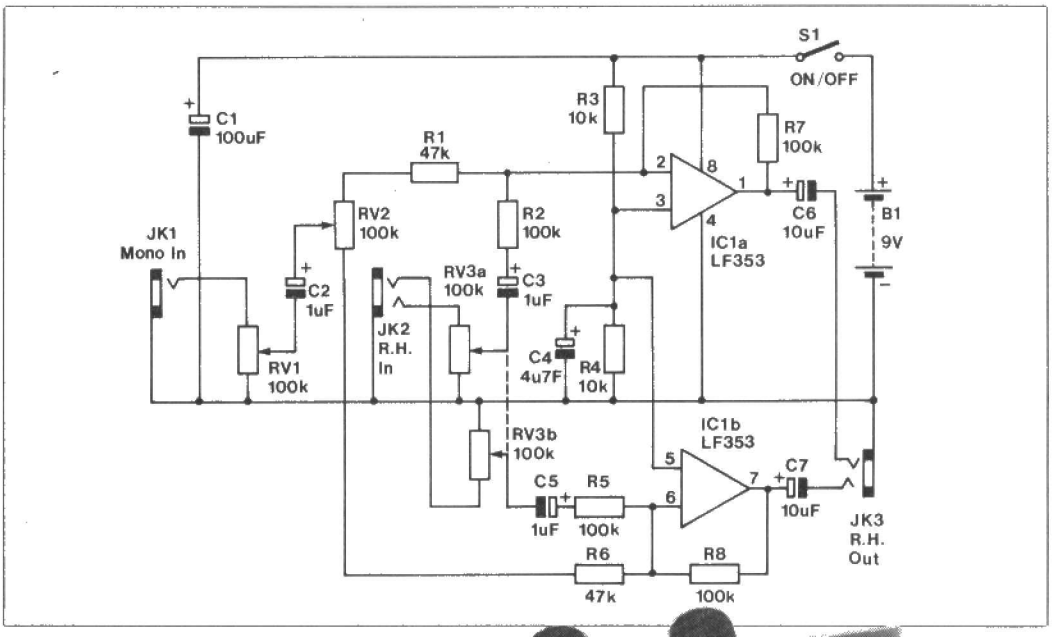


Figure 3. Circuit

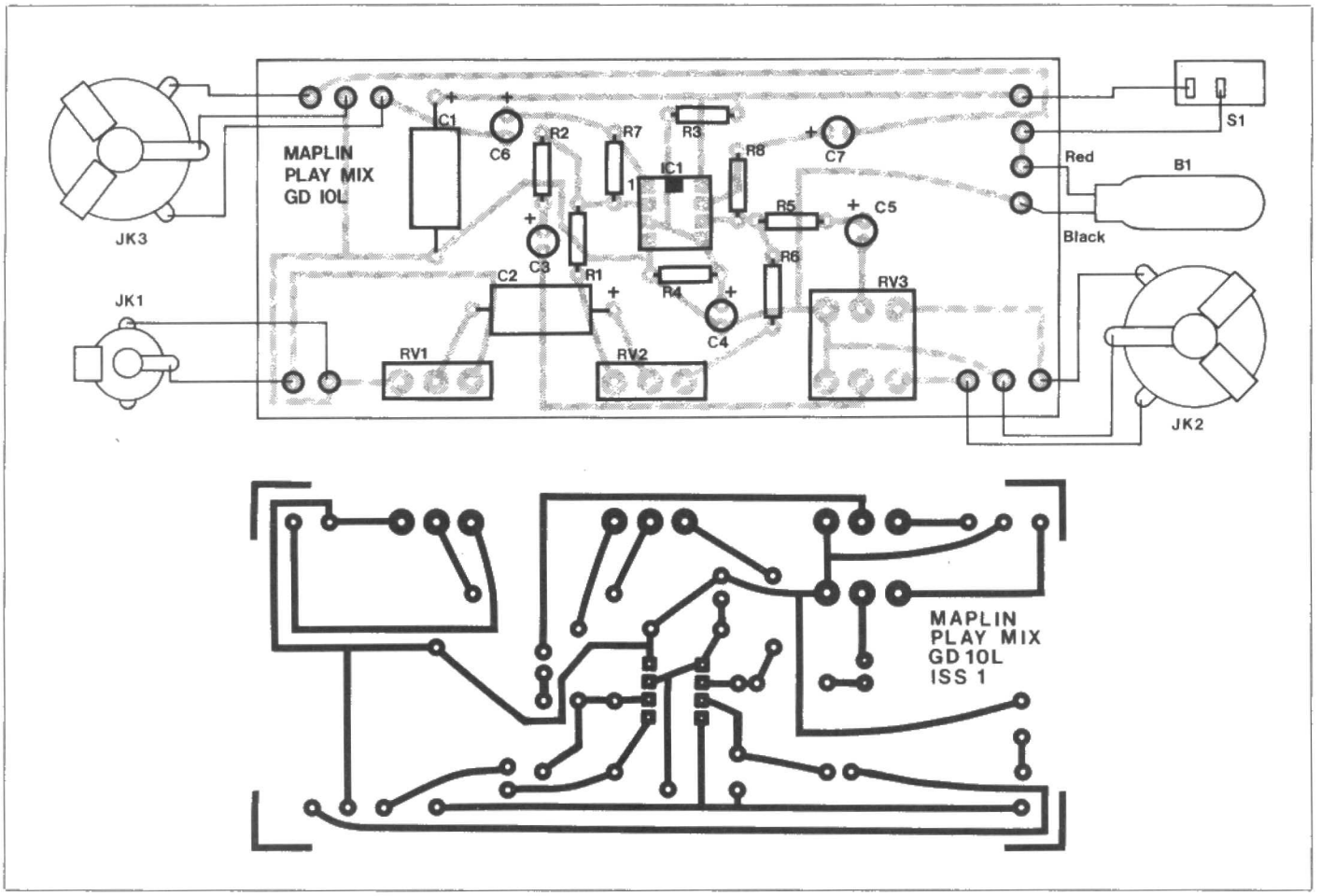


Figure 4. PCB Layout and Wiring

must also provide isolation between the two outputs so that one does not end up driving the other (which could result in distortion or even damage to one of the outputs). The input resistors would normally have a fairly high value which would prevent this, but almost total isolation is provided by the 'virtual earth' at the inverting input. Obviously, this point in the circuit is not connected to earth but, depending on the circuit design, the feedback action maintains it at earth potential or at some fixed offset from earth potential, and this blocks any signal flow from one input to the other.

Circuit Operation

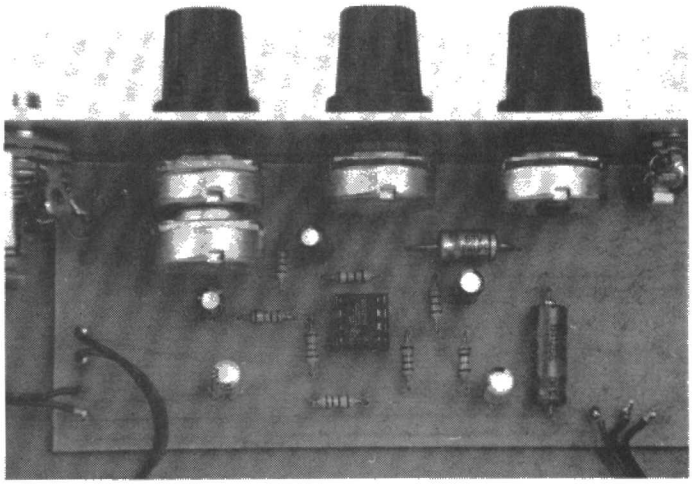
The full circuit diagram of the mixer appears in Figure 3. The two mixer circuits bear an obvious resemblance to the basic configuration of Figure 2, and the main difference is the addition of DC blocking capacitors at the inputs and output of each one. Also, a common potential divider bias circuit is used for the two mixers, and this circuit includes decoupling capacitor C4. RV3 is the dual gang level control at the stereo input, and RV1 is the mono (instrument) gain control. The 'pan' control is RV2, and this acts as part of the input resistance for the mono input of each channel. With RV2 at a central setting the input resistance for each channel is the same at 97k, giving roughly unity gain through the mixer. Offsetting RV2 gives a higher input resistance in one channel, with reduced gain, while there is reduced resistance and higher gain in the other channel. Each channel can be boosted by around 10dB relative to the other channel, which is sufficient to permit the instrument to be positioned anywhere in the stereo sound stage.

The device specified for IC1 is a Bifet type which uses Jfet transistors to achieve very low noise and distortion levels. An inexpensive bipolar dual operational amplifier such as the 1458C will also work quite well in the circuit though. The current consumption is only about 3.5 milliamps, and even a small (PP3 size) 9 volt battery will give many hours of operation.

Construction

Apart from the sockets and battery, all the components fit onto the printed circuit board. Details of the track pattern and component layout are provided in Figure 4.

The only unusual aspect of



construction is the use of printed circuit mounting potentiometers, and obviously you must make sure you obtain the correct type. The printed circuit board is effectively mounted on the front panel of the case via these components. If preferred, ordinary potentiometers can be used, but these would have to be hard-wired to the printed circuit board. The board would then have to be bolted in place on the base panel of the case, and there are plenty of vacant areas on the board which could accommodate the mounting holes. When fitting the potentiometers, make sure that they are fully pushed down into place before making the soldered connections, and use plenty of solder to ensure that physically strong joints are produced. Fit pins to the board at the points where connections to the battery, sockets, and on/off switch will be made.

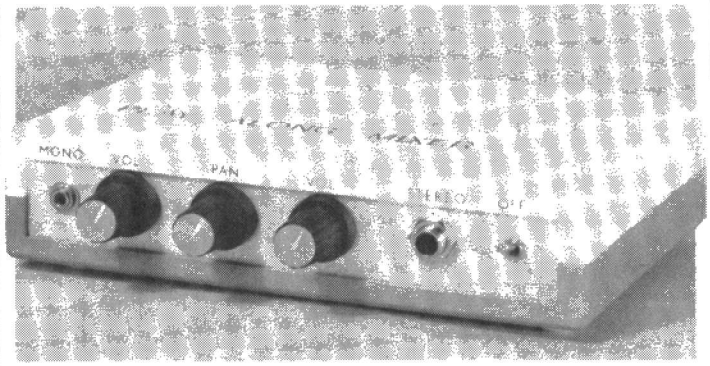
On the prototype JK1 is a 3.5mm jack, while JK2 and JK3 are standard stereo jacks. These could be changed for other types that would be more convenient in your particular set-up, with the only proviso being that you must be sure that sufficient space is available for the proposed types of socket. A verocase having approximate outside dimensions of 180 by 120 by 39 millimetres is used as the housing for the

prototype. This is quite tough and gives a neat appearance, but care has to be taken with the layout as it has barely enough height to take the printed circuit assembly. The controls must be mounted a millimetre or two above the centre-line of the panel, and if the pins of the potentiometers protrude by a substantial amount on the underside of the board, it might be necessary to trim these down slightly. Some of the mounting pillars moulded into the case might tend to get in the way, but these can easily be drilled away using a bit of around 10 millimetres in diameter.

To complete the unit, the battery clip is connected and S1 plus the three sockets are wired to the printed circuit board. Ordinary connecting wire is adequate for the connections to the sockets and it is not essential to use screened cable here.

In Use

If the programme source is separate from the amplifier, in most cases the mixer will simply connect between the cassette deck, tuner, or other source, and the amplifier, using screened leads. The exception is where the unit is to be used with a record deck as the signal source. The output from a cartridge is not adequate to drive the mixer properly, and a suitable pre-amplifier would have to be added ahead of the mixer. In many cases the preamplifier in the receiver or amplifier can be used, with the mixer being connected between the 'preamp out' and 'power amp in' sockets, or perhaps being fitted into the tape monitor facility. This is something that varies from one hi-fi amplifier to another, and the method of connection must be varied to suit the particular equipment you are using. Reference to the amplifier's manual should help if you are uncertain about a suitable method of connection. If you have some form of integrated audio system such as a tuner/amplifier or a casseiver unit, there will probably be input/output sockets into which the mixer can be connected, or a tape monitor facility might again be the answer. It is only possible to use the mixer if there is some means of routing the output of the programme source through the mixer and into the power amplifier.



Results will probably be best with RV3 set at maximum, and RV1 set to mix in the instrument at the required level. RV3 can be backed off if there is any sign of overloading, or if the instrument cannot be brought up to a satisfactory level even with RV1 set at maximum. RV2 is, of course, set to place the instrument at the desired position within the stereo field.

If the instrument gives only a low output level it might be necessary to modify a few component values in order to boost the gain at the mono input and give an adequate signal level at the output. This simply entails raising R2, R5, R7 and R8 to about 1M in value. With something like a very low output guitar pick-up it would probably be better to drive the mixer via a pre-amplifier rather than try to modify the values to boost the gain at the mono input to a suitable level.

PLAY ALONG MIXER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,6	47k	2	(M47K)
R2,5,7,8	100k	4	(M100K)
R3,4	10k	2	(M10K)
RV1	100k Pot Log	1	(FW25C)
RV2	100k Pot Lin	1	(FW05F)
RV3	100k Dual Pot Log	1	(FX12N)
CAPACITORS			
C1	100µF 10V Axial Electrolytic	1	(FB48C)
C2	1µF 100V Axial Electrolytic	1	(FB12N)
C3,5	1µF 100V PC Electrolytic	2	(FF01B)
C4	4µ7F 63V PC Electrolytic	1	(FF03D)
C6,7	10µF 50V PC Electrolytic	2	(FF04E)
SEMICONDUCTORS			
IC1	LF353	1	(WQ31J)
MISCELLANEOUS			
	PC Board	1	(GD10L)
	DIL Socket 8 pin	1	(BL17T)
	Veropins 2145	1 Pkt	(FL24B)
S1	SPST Ultra-Min Toggle	1	(FH97F)
JK1	Jack Socket 3.5mm	1	(HF82D)
JK2,3	Stereo Open Skt.	2	(HF93B)
	Knob Cap Blue	3	(QY01B)
	Battery Clip PP3	1	(HF28F)
	Case Verobox 214	1	(LQ07H)
	Wire Hook up	1 Pkt	(BL00A)
	Knob	3	(YG40T)

A complete kit of parts is available for this project:
Order As LK93B (Play Along Mixer Kit) Price £13.95
The following item in the above kit list is available separately and is not shown in our 1986 catalogue:
Play Along Mixer PCB **Order As GD10L Price £1.95**

MAPLIN'S TOP TWENTY KITS

THIS MONTH	LAST	DESCRIPTION OF KIT	ORDER CODE	KIT PRICE	DETAILS IN PROJECT BOOK
1.	(2)	75W Mosfet Amplifier	LW51F	£15.95	Best of E&MM
2.	(1)	Live Wire Detector	LK63T	£2.95	14 (XA14Q)
3.	(3)	Car Burglar Alarm	LW78K	£7.45	4 (XA04E)
4.	(6)	Partylite	LW93B	£9.95	Best of E&MM
5.	(5)	Ultrasonic Intruder Detector	LW83E	£10.95	4 (XA04E)
6.	(7)	8W Amplifier	LW36P	£4.95	Catalogue
7.	(18)	PWM Motor Driver	LK54J	£9.95	12 (XA12N)
8.	(4)	Logic Probe	LK13P	£12.95	8 (XA08J)
9.	(12)	U/Sonic Car Alarm	LK75S	£17.95	15 (XA15R)
10.	(14)	Syntom Drum Synthesiser	LW86T	£12.95	Best of E&MM
11.	(17)	15W Amplifier	YQ43W	£5.75	Catalogue
12.	(11)	Light Pen	LK51F	£8.95	12 (XA12N)
13.	(–)	Stppr Motor & Driver	LK76H	£12.95	Catalogue
14.	(16)	Burglar Alarm	LW57M	£49.95	2 (XA02C)
15.	(13)	Harmony Generator	LW91Y	£17.95	Best of E&MM
16.	(15)	ZX81 I/O Port	LW76H	£9.95	4 (XA04E)
17.	(–)	150W Power Amp	LW32K	£21.95	Catalogue
18.	(–)	Programmable Timer	LW98G	£7.95	1 (XA01B)
19.	(9)	Computadrum	LK52G	£9.95	12 (XA12N)
20.	(–)	80m Converter Receiver	LK41U	£18.95	10 (XA10L)

Over 100 other kits also available. All kits supplied with instructions.
The descriptions above are necessarily short. Please ensure you know exactly what the kit is and what it comprises before ordering, by checking the appropriate Project Book mentioned in the list above.

MACHINE CODE PROGRAMMING WITH THE Z80

Z80

by Graham Dixey C.Eng., M.I.E.R.E. Part 1

The Z80, like the 6502, has been with us for some time now and, in spite of rising stars like the 16-bit and 32-bit processors, will be with us for a long time yet. There are numerous machines, actually hundreds of thousands, that use this powerful 8-bit chip and presumably, a good number of their owners who, for one reason or another, have not yet mastered machine code. There is, indeed, the widespread fear that machine code programming is terribly difficult and quite beyond the average mortal. Nothing could be further from the truth. It does require a fair degree of application to get to grips with it but surely anyone keen enough to learn has this already. In a word, it comes down to 'motivation'. This new series will look at the Z80, its architecture and instruction set and will show by example how to exploit the infinite capabilities of this processor and its related support chips. It will assume that readers already have some idea of hexadecimal numbers (from here on known as HEX) but will give you gentle nudges in the ribs from time to time when HEX arithmetic is encountered. In addition to this, for the benefit of those who need a little more information on some fundamental ideas that will arise from time to time, there is a section at the end of this article called 'Back to Basics' which will explain these points. This means that the main text will not be broken into every time that such explanations are needed and those that do not need them will be able to ignore them and read on.

Different readers have different reasons for wanting to learn to use machine code. Maybe they want to control the physical environment in some way, which will involve receiving signals in some form, perhaps just switched inputs, but maybe also analogue signals converted to digital form in an A-D converter. Then processing such signals and outputting others to operate motors, lamps, relays, etc. In other words, the computer is being used in a real-time engineering application. Others may want to know how to use machine code to speed up program operation since it is well known that the best graphics programs (e.g. games) run faster when written in machine code than when in BASIC. Both wishes will be met within the constraints of space. It is hoped that 'Machine Code Programming with the Z80' will unlock doors previously barely opened or even shut fast.

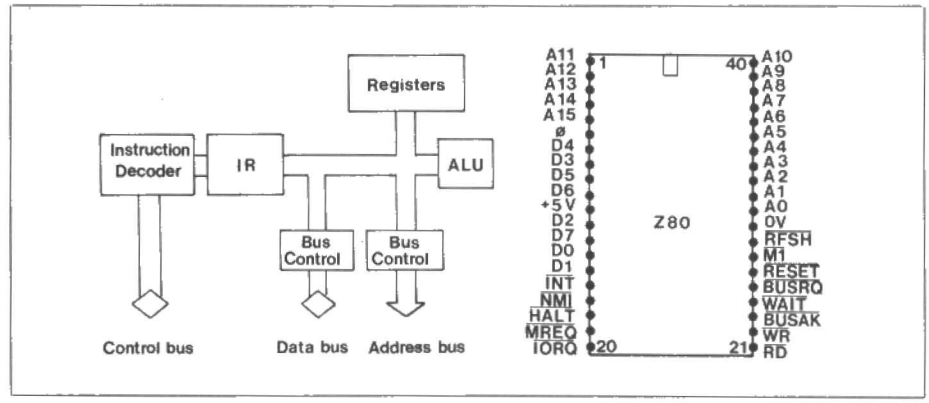


Figure 1. Z80 Architecture and Pin-out.

Main set		Alternate set		
A	F	A'	F'	General purpose register group
B	C	B'	C'	
D	E	D'	E'	
H	L	H'	L'	
Interrupt vector I		Memory refresh R		Special purpose register group
Index register IX				
Index register IY				
Stack pointer SP				
Program counter PC				

Figure 2. The Z80 Register Set.

Introducing the Z80

Figure 1 shows the main blocks found within the Z80 chip. The programmer's primary concern is with the block marked registers but a few clarifying remarks on the other blocks would not be amiss.

First, the ALU or Arithmetic/Logic Unit. This could be said to be the 'computing heart' of the chip since it is here that the actual arithmetic and logical functions are carried out. In other words, this is where the data is processed. For example, when adding the contents of two registers together, these contents will be input to the ALU on receipt of an ADD instruction and the result will be deposited in one of the registers.

A register vital to any microprocessor but not accessible to the programmer, is the Instruction Register (IR). During the course of a program, the instructions from memory are held here, one at a time, while they are decoded. This is carried out by the next block to the left. Suppose, for example, that the HEX digits 3A have been fetched from memory and are in the IR. These digits have a specific function which must be identified. The decoding process reveals to the Z80 that this is an instruction 'to load the A register with data from a memory location that will be specified by the next two bytes of data found'. This sounds a bit long-winded and naturally, the Z80 does not think in quite these terms any more than we think directly in machine terms. Nonetheless, the result of decoding this byte is to prepare the A register to receive data that will now be fetched from a given memory location.

As already stated, the registers are of prime importance to the programmer. They fall into three main classes which are listed below and shown in Figure 2.

The Main Register Set
The Alternate Register Set
The Special Purpose Registers

These registers will be discussed in some detail shortly.

Control functions will not be discussed at this stage since this will serve little purpose other than to cloud the issue. They will be introduced in context when and if required. Figure 1 also shows the pin-out of the Z80 which, if it does nothing else, does enable one to identify the 8-bit data bus, the 16-bit address bus and the profusion of control lines that comprise the control bus. It also shows the power supplies (+5V, 0V) and the clock 0, whose function is to synchronise system operation and which is nothing more than a precise and stable crystal-controlled oscillator.

The Main Register Set

All the registers in this set are 8-bits 'wide'. The set comprises an accumulator (A), often known just as the A register, a 'flags' register (F) and six general purpose registers (B,C,D,E,H and L).

The Alternate Register

This is nothing more than a 'carbon copy' of the main register set, each register being distinguished by the prime (′). Thus the equivalent of the main register set's A register is known in the alternate set as the A′ register. In general, the arithmetic and logical operations are performed on data in the A registers but the other general purpose registers have their uses too, as will be evident as the series unfolds.

Flag Registers (F and F′)

Terms used in computing often have parallels in quite unrelated fields. Flags is an obvious one. Conventionally a flag is a signal; the flag may be 'up' or 'down' to indicate one of two possible states, just like bits that are either 1 or 0. In the flags register, each bit is an individual flag that may be 'up' (SET or equal to 1), or 'down' (CLEAR or equal to 0). In the same way that a person may look at a flag to see if it is OK to proceed with some operation or other, so the program will test the status of a flag (see if it is SET or CLEAR) in order to arrive at a decision. Flags are used as the basis for what are known as conditional jumps, of which more later.

As for the flags themselves, there are six of them and they are shown in Figure 3.

The carry flag (C) can be set by an addition operation, for example, when adding two 8-bit numbers producing a 9-bit result. The following example shows this happening:

```
  11010101
+ 10100010
-----------
 101110111
 ↑
 9th bit (carry out)
```

The 9th bit is obviously part of the result but, with 8-bit registers, can obviously drop off the end unless there is

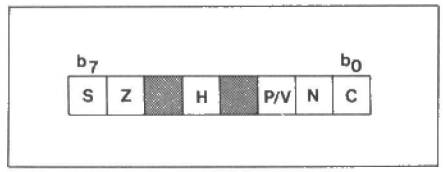


Figure 3. The 'Flags' Registers F and F′.

something there to catch it! This catching operation is performed by the carry flag which acts as a temporary store.

The zero flag (Z) echoes the state of the A register, following some operation, as to whether its contents are zero or non-zero. If A is zero, then Z = 1, but if A is non-zero, then Z = 0. A very useful flag this one, as it allows us to escape from loops at given moments.

The sign flag (S) is used with two's complement arithmetic (see Back to Basics) and tells us if the A register contents are positive (S = 0) or are negative (S = 1).

The function of the parity/overflow flag (P/V) is two-fold. After a logical operation (AND, OR, EXCLUSIVE OR) it indicates the parity of the result. After two's complement arithmetic, it tells us whether an overflow has occured. Overflows affect the validity of the result of such arithmetic and must be detected. Both parity and overflows are explained in 'Back to Basics'. The P/V flag is set for even parity or when an overflow occurs. Consequently, it is clear for odd parity or if there is no overflow.

There are two flags that are used in BCD arithmetic. One is the half-carry flag (H), which indicates the BCD carry or borrow result from the low to the high 'nibble' of an 8-bit addition or subtraction. This flag is used by the Decimal Adjust instruction, as we shall eventually see, but because the method of use of this instruction is different for addition and subtraction, we need to look at the Add/Subtract flag (N) to find out what the last operation in the A register was.

One important point before we leave the flags register. Note that the flags are affected by arithmetical and logical operations, but NOT by register loading operations. For example, a subtraction in the A register that gives a negative result will set the sign flag to indicate that this is a negative result, but loading a positive number into the A register immediately afterwards *will not* clear the flag.

The Register Pairs

It was not just coincidence or for convenience of drawing that the registers are arranged as they are in Figure 2. Below A and F (and hence below A′ and F′) the registers are set out in pairs BC, DE, HL (B′C′, D′E′, H′L′). This pairing provides us with the facilities of 16-bit arithmetic and the use of an addressing mode known as 'register indirect'.

The Special Purpose Registers

There are six of these special purpose registers and the first one we will consider is the program counter (PC). This is a 16-bit register and since it is possible for each bit to be in either the 1 or 0 state, this gives us 2^{16} possible states of this register, which is 65,536 or 64k (since 1024 = 1k). From this conclusion you may not be surprised to learn that the program counter keeps track of the memory addresses as the program runs. In fact, it is the program counter that 'guides' the computer through the required program sequence. At the beginning, it is loaded with the start address of the program and as the program runs, it is incremented to access all the instructions and data in the required sequence. When jumps have to be made or there are 'interrupts', it is the PC that is loaded with a new address so that we can access some other area of the program.

Registers IX and IY are 16-bit index registers and are used in the 'indexed addressing' mode, of which more in good time.

The register known as SP is the stack pointer register and a brief explanation of what we mean by the 'stack' would not be out of place.

The stack is a reserved area of RAM, not for entering our programs into, but to act as short term storage for data that might otherwise get lost. How could this situation arise? Well if, without actually describing what we mean by an interrupt in detail, we can accept that a program running can be interrupted by another program, then we can begin to see why we need a stack. Suppose that the interrupting program needs to use the A register. It is likely that the main program has also been using this register and has essential data in it. If it is just handed over to the interrupting program, then this data will be lost. As a result, when we return to the main program, it will have been corrupted. Not only the A register might be involved, but others too. An obvious one is the program counter, since the interrupting program will reside elsewhere in memory. If we don't note where we were when the program was interrupted, how can we know where to return to after the interrupt? The answer is to 'push' the contents of all the affected registers onto the stack at the beginning of the interrupt and 'pull' them off again when it finishes and then the main program can continue as if nothing had happened.

The next register is the Interrupt Page Address Register (I), which is used when the Z80 is working with peripherals. Further details are better left until later. The final register is the refresh register (R), which the Z80 uses when it is supplied with dynamic memory. In this type of memory, data is stored as an electric charge on the minute capacitance of MOS transistor gates. Because this charge tends to leak away relatively quickly, it has to be kept topped up or 'refreshed'. This is carried out periodically by 'on chip logic' and the programmer is totally unaware of the operation.

That completes our brief survey of

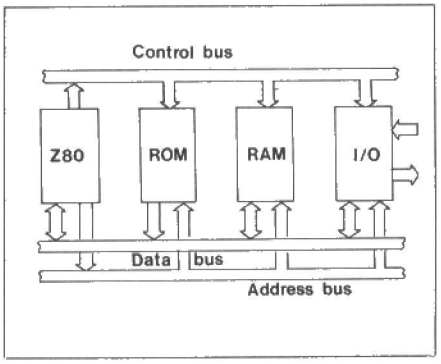


Figure 4. Essential Main Blocks of a Microcomputer.

the Z80 architecture. We now know that we shall be mainly concerned with a set of registers and that the function of the instruction set is to allow us to move data round between these registers and memory and carry out certain processes on it as required. Each instruction, by itself, is usually quite simple to understand. The trick is knowing which instructions to use to achieve a given goal. Now it's time to take a look at what we call 'memory addressing'.

Memory Addressing

Let's define what we mean by this. Any microcomputer can be represented by just four main blocks, as shown in Figure 4. The microprocessor itself, in this case the Z80, will be one of these blocks; the ROM (containing various monitor routines, BASIC interpreter, etc) will be another; then there will be the RAM (for our own user programs) and finally, there will be the input/output ports (I/O) since without these, there can be no contact with the outside world; not even with a keypad or display!

Every location in either ROM or RAM and the input/output ports themselves will have their own addresses. By specifying which addresses we want to use, we can tell the Z80 where to go for data, where to get data from, and so on. Memory addressing is the general term for this and because there are a variety of ways in which it can be done, we have the concept of addressing modes. Also, we sometimes want to shift data between registers within the Z80 rather than with RAM or I/O. There will be addressing modes for this too. These modes will be the next topic for discussion.

One thing that can be a little confusing at first is that different modes of addressing may occupy one, two, three or even four bytes. What this means is that some instructions need only a single memory location to store them, others need up to four locations. Once you get used to looking up the machine code 'op codes' the problem largely disappears. But keep this byte format in mind as you read on through the various modes.

Register Addressing

This mode is used where operations are confined to data held in the registers. An example is where the contents of one register are to be loaded into another. The following instruction LD A,B is an example and is said to be in mnemonic form or, as it's usually called, assembler format. The letters LD stand for 'load' and represent the mnemonic for this particular instruction. The advantage of mnemonics is their ease of recognition in contrast with the HEX digits of their machine code equivalents into which they have to be ultimately assembled. Coming back to LD A, B this means 'load register A with the contents of register B'. Note that the destination, A, is specified *before* the source B.

Register addressing needs only one byte, e.g. for the above instruction it is 78 in HEX.

Immediate Addressing

This mode is a very easy one. It is used where the operation uses some fixed value of data. For example, 'add the number 5 to register A'. This needs two bytes, which is obvious when you think about it, because one byte must be for the op code and the other for the number. For the case quoted, the machine code instruction would look like this:-

C6 05

The op code for 'add anything to the A register' is C6 and 05 is how we enter the number 5 into the program.

Extended Addressing

This mode of addressing allows us access to contents of RAM locations. When we remember that the addresses are all sixteen bits long and this is two bytes, then it seems entirely logical that to access the contents of memory location 0D1A, for example, we should need two bytes for the address in addition to any bytes needed for the instruction itself. Since these instructions can take either one or two bytes, then extended addressing will always take three or four bytes.

Suppose that there was a sub-routine starting at location 0D1A that we wished to call. The op code for this sub-routine call is CD so that the instruction line in machine code will look like this:-

CD 1A 0D

It may surprise you to see that the address is written 'low byte first'. This is a golden rule that must always be obeyed.

Immediate Extended Addressing

Suppose we are working with 16-bit data (i.e. two bytes) and we wish to load it into memory (needing, therefore, two successive memory locations), or we wish to load a 16-bit number into an index register or register pair such as B,C. Since we are dealing with fixed data, this is obviously 'immediate' mode, but will need two bytes to specify the data so is 'extended' as well. In this mode, the op code will occupy one or two bytes and the data always two bytes, giving a total instruction length of either three or four bytes. To take an example, we wish to load the number 2F05 into the register pair B,C. The op code for this load is 01, so the machine code instruction looks like this:–

01 05 2F

Please note again the convention that the 16-bit data is entered 'low byte first'.

Register Indirect Addressing

In this mode, a register pair, BC for example, are used as a 'pointer' for where data is to be found for, say, another register to use, such as the A register. What we mean by a pointer is that the register pair in question, being two bytes altogether, is able to hold an address at which the data may be found. Suppose we wish to store the contents of the A register in memory location 0C35, then we should first load a register pair with this address and then use the appropriate op code to instruct the A register to load its contents into this address.

Indexed Addressing

This mode, which is a form of register indirect addressing, is a very useful one when it is desired to access tables of data in memory. There are two index registers, IX and IY which, as mentioned earlier, are sixteen bit registers. Thus, they can be loaded with an address which will be known as the 'base address'. The mode specifies a displacement, usually denoted by 'd' which is 'signed', i.e., is in two's complement form so that it can represent positive or negative numbers. This needs an example to make it clear so consider that the base address is 0320. If 'd' = 06 (i.e. +6), then the index register will access the address obtained by taking the sum of 0320 + 06 = 0326. 'So what?', you say, why not use this value in the first place? A fair question and the answer is that 'd' can be made to change, usually in steps of one (either incrementing or decrementing) and so goes through a whole consecutive range of addresses. Remember the data table that I mentioned earlier? Well, that's how we obtain access to its contents.

Indexed addressing always uses a two byte op code followed by a single byte displacement.

Relative Addressing

This mode is used only for jumps. We decide where we want to jump to in a program (jumps are rather like GOTOs in BASIC), work out how many steps are needed to get there and that is our displacement 'e' that must be added to the 'start' address. This start address is the current address (the one holding the jump instruction) + 2. Suppose the jump instruction is stored at memory location 0250 and we wish to jump forward to 025A, then the start address is 0250 + 2 = 0252. To get to the destination for the jump 025A, we need to go eight steps on, so 'e' = 08.

Modified Page Zero Addressing

The eight instructions that use this mode are all sub-routine calls to the 256 addresses in the range 0000 – 00FF (Page Zero). These calls are known as 'restarts' and are a neat way of calling frequently used sub-routines.

Implied Addressing

Any instruction that doesn't need an address or data (an operand in other words), uses this mode. Complementing the carry flag is an example. The mode is also known as 'implicit'.

Bit Addressing

This mode allows the testing of the individual bits in a register or memory location. Its value is that it can utilise these bits as if they were user-defined flags, telling us if an input switch is closed (engineering application) or the gender of a member of staff in a file (business application). Individual bits can also be set or reset as required using this mode.

Well, that completes our survey of the Z80 addressing modes. Unless you're either a genius or have done it before, they won't all have sunk in entirely. Don't worry, it's not a memory test. They're there for reference and I shall use them all in practical examples in due course.

Now, for those who need a bit of a brush-up in the fundamentals, it's:

Back to Basics

Denary, Binary and Hexadecimal Numbers

These three number systems have got to become almost second nature if you're going to program in machine code. Fortunately, they're very easy to pick up once you grasp the basic idea. This is that any number, in whatever system, is a series of digits which are 'coefficients' (i.e. multipliers) and the value of the number is simply obtained by multiplying each coefficient by the 'weighting' of the column in which it appears. The terms are worse than the facts. The weightings of the columns in denary (decimal) are what we were first told about numbers, that is ones, tens, hundreds, thousands, etc. Nothing strange or difficult about that, is there? Look at the following denary number and apply this idea to it.

2638
= (2 x thousands)
+ (6 x hundreds)
+ (3 x tens)
+ (8 x ones)

Now consider the binary system which works on exactly the same principle except that it goes in steps of 2, not 10. In other words, the weightings are 1, 2, 4, 8, 16, 32, 64, 128, etc. These are the first eight weightings and these are worth remembering because our data is often in eight bit 'words'. Now take an example. This is going to be easier than denary because the coefficients will always just be 1 or 0. For example:-

10011011
= (1 x 128)
+ (0 x 64)
+ (0 x 32)
+ (1 x 16)
+ (1 x 8)
+ (0 x 4)
+ (1 x 2)
+ (1 x 1)
= 128 + 16 + 8 + 2 + 1
= 155 (in denary)

Note that what I have actually done is to write down an example of a binary number and then, by using the column weightings for each bit, show how to evaluate its equivalent denary value.

Finally, we have the hexadecimal system which does look unfamiliar because not only does it use the digits 0 – 9 but also the letters A – F. This is necessary because it is a 'base 16' system (compared with denary which is base 10 and binary which is base 2). Therefore, it has to have 16 digits, and as only ten numerical figures exist, it extends to the first six letters, A – F, of the alphabet which represent the other six. The digits 0 – 9 mean exactly the same thing in hexadecimal as they do in denary but from there on, we have as follows:–

A = 10
B = 11
C = 12
D = 13
E = 14
F = 15

Because the base is so large, the column weightings quickly become unwieldy but, fortunately, this doesn't bother us. The first four column weightings are:

1; 16; 256; 4096

To take an example of a four-digit hexadecimal number and its denary equivalent, consider 2C3A. This equals:–

(2 x 4096)
+ (C x 256)
+ (3 x 16)
+ (A x 1)
= 8192 + 3072 + 48 + 10
= 11322

As an example for yourselves, try evaluating the largest four bit hexadecimal number which is FFFF. You shouldn't be surprised at the result, especially when it's divided by 1024!

Converting binary to hexadecimal is easy. Each hexadecimal digit can be represented by a four bit binary group. For example, 0 = 0000 and F = 1111 with all the other digits in between. With 8-bit data or 16-bit addresses, we end up with either TWO or FOUR hexadecimal digits respectively. Thus the binary number 10011011 splits into two 4-bit groups (known as 'nibbles') which are 1001 and 1011, which are respectively 9 and 11 (B). Thus, the hexadecimal equivalent of 10011011 is 9B. Try writing the hexadecimal number 3AF6 in binary as a self-test. You should get 0011101011110110.

Two's Complement Numbers

These arise because of the need to be able to represent both positive and negative numbers using only binary 1 and 0. With 8-bit numbers, the leftmost bit (the Most Significant Bit or bit-7 as it's often known) is always 0 for positive numbers and 1 for negative numbers.

From this, we can see that the largest 'signed' positive number is 01111111, which equals 127 (denary). The next number in the series is 10000000 which is actually −128 as you'd expect. The question is 'how do you represent small negative numbers such as −1? Is that 10000001?' The answer is no! The method is to write it in two's complement form. Space considerations preclude a detailed discussion of this idea but I will show the mechanics of it. First accept that, with 8-bit data, the largest negative number you can have is −128. Now, take any number from −1 to −128. Suppose we say −4.

First of all, write this as an 8-bit binary number:

= 00000100

Now 'invert' all the bits (swap 1s and 0s):

= 11111011

Now add 1 to the least significant bit:

= 11111100 (1011 + 1 = 1100)

This is now in two's complement form. Because we usually want to write it in hexadecimal, encode the two nibbles thus; 1111 = F; 1100 = C. Therefore −4 in hexadecimal is FC. Try an example. Try putting −1 into 'signed hexadecimal'; the answer is FF.

Parity

There are two types, 'even', in which the number of 1's in a byte is an even number, and 'odd', in which the number of 1's in the byte is odd. It is a method of error checking in data transmission and more than that need not be said at the moment.

Overflows

Overflows in arithmetic cause errors and need detecting. The definition of an overflow is when a carry takes place from bit 6 into bit 7, giving rise to an incorrect sign in the result. That is, an answer that should have been positive becomes negative and vice-versa. It is usually the result of using data that is 'out of range' of the permitted size of numbers.

And Finally

I've no doubt that this opening part to the series will have given you something to digest. It certainly has laid a lot of ground work which means that we can get down to the real task of programming next time. If you're too impatient to do nothing else until then, get a copy of 'A Z80 Workshop Manual' by E.A. Parr, published by Bernard

DESTINATION	SOURCE																		
		IMPLIED		REGISTER							REG. INDIRECT			INDEXED		EXT. ADD.	IMM
		I	R	A	B	C	D	E	H	L	(HL)	(BC)	(DE)	(IX+d)	(IY+d)	(nn)	n
REGISTER	A	ED 57	ED 5F	7F	78	79	7A	7B	7C	7D	7E	0A	1A	DD 7E d	FD 7E d	3A n n	3E n
	B			47	40	41	42	43	44	45	46			DD 46 d	FD 46 d		06 n
	C			4F	48	49	4A	4B	4C	4D	4E			DD 4E d	FD 4E d		0E n
	D			57	50	51	52	53	54	55	56			DD 56 d	FD 56 d		16 n
	E			5F	58	59	5A	5B	5C	5D	5E			DD 5E d	FD 5E d		1E n
	H			67	60	61	62	63	64	65	66			DD 66 d	FD 66 d		26 n
	L			6F	68	69	6A	6B	6C	6D	6E			DD 6E d	FD 6E d		2E n
REG. INDIRECT	(HL)			77	70	71	72	73	74	75							
	(BC)			02													
	(DE)			12													
INDEXED	(IX+d)			DD 77 d	DD 70 d	DD 71 d	DD 72 d	DD 73 d	DD 74 d	DD 75 d							DD 36 d n
	(IY+d)			FD 77 d	FD 70 d	FD 71 d	FD 72 d	FD 73 d	FD 74 d	FD 75 d							FD 36 d n
EXT. ADD.	(nn)			32 n n													
IMPLIED	I			ED 47													
	R			ED 4F													

Table 1. 8-Bit Loads (LD).

DESTINATION	SOURCE											
		REGISTER							IMM. EXT.	EXT. ADD.	REG. IND.
		AF	BC	DE	HL	SP	IX	IY	nn	(nn)	(SP)
REGISTER	AF										F1
	BC								01 n n	ED 4B n n	C1
	DE								11 n n	ED 5B n n	D1
	HL								21 n n	2A n n	E1
	SP				F9		DD F9	FD F9	31 n n	ED 7B n n	
	IX								DD 21 n n	DD 2A n n	DD E1
	IY								FD 21 n n	FD 2A n n	FD E1
EXT. ADD.	(nn)		ED 43 n n	ED 53 n n	22 n n	ED 73 n n	DD 22 n n	FD 22 n n			
REG. IND. (Push)	(SP)	F5	C5	D5	E5		DD E5	FD E5			(Pop)

Table 2. 16-Bit Loads (LD, PUSH & POP).

		IMPLIED ADDRESSING					
		AF'	BC' DE' HL'	HL	IX	IY
IMPLIED	AF	08				
	BC DE HL		D9 (EXX)			
	DE			EB		
REG. INDIRECT	(SP)			E3	DD E3	FD E3

N.B. All op codes except D9 refer to mnemonic EX.
Op code D9 refers to mnemonic EXX.

Table 3. Exchanges (EX & EXX).

DESTINATION	SOURCE		
		REGISTER INDIRECT	
		(HL)	MNEMONIC
REGISTER INDIRECT	(DE)	ED A0	LDI
		ED B0	LDIR
		ED A8	LDD
		ED B8	LDDR

Register HL points to source.
Register DE points to destination.
Register BC is a counter.

Table 4. Block Transfer Group.

SEARCH LOCATION	
REGISTER INDIRECT	
(HL)	MNEMONIC
ED A1	CPI
ED B1	CPIR
ED A9	CPD
ED B9	CPDR

HL points to memory location where data is to be compared with contents of register A. BC is a counter.

Table 5. Block Search Group.

Babani at £2.95. In these days of high prices for books, this is incredibly good value and thoroughly recommended. You can get a copy from Maplin (order as WA54J) but add 50p for handling.

Though the series is being written for the benefit of any one owning a Z80-based machine, the recently available Maplin Z80 CPU card will be developed both in terms of software and hardware for those who want to build a system from scratch.

The Z80 Instruction Set

In the following tables, certain conventions have been adopted. These are listed below:

(a) A, B, etc, means the register A, the register B, etc.
(b) BC means the 'contents' of the register pair BC.
(c) (BC) means the contents of the memory location 'pointed to' by the address held in the register pair BC.
(d) n means the 'literal' or single-byte number n.
(e) nn means the two-byte number nn.
(f) (nn) means a two-byte address nn, the low byte of this address being specified first.
(g) d is a 'signed displacement' added to an index register e.g. (IX+d), IY+d), forming an address pointer.
(h) e is a signed displacement used in relative addressing.

		SOURCE						
MNEMONIC	DEST.	BC	DE	HL	SP	IX	IY
ADD	HL	09	19	29	39		
	IX	DD 09	DD 19		DD 39	DD 29	
	IY	FD 09	FD 19		FD 39		FD 29
ADC	HL	ED 4A	ED 5A	ED 6A	ED 7A		
SBC	HL	ED 42	ED 52	ED 62	ED 72		
INC		03	13	23	33	DD 23	FD 23
DEC		0B	1B	2B	3B	DD 2B	FD 2B

Table 7. 16-Bit Arithmetic & Logic.

	SOURCE									
	REGISTER ADDRESSING							REG. IND.	INDEXED		IMM.
MNEMONIC	A	B	C	D	E	H	L	(HL)	(IX + d)	(IY + d)	n
ADD	87	80	81	82	83	84	85	86	DD 86 d	FD 86 d	C6 n
ADC	8F	88	89	8A	8B	8C	8D	8E	DD 8E d	FD 8E d	CE n
SUB	97	90	91	92	93	94	95	96	DD 96 d	FD 96 d	D6 n
SBC	9F	98	99	9A	9B	9C	9D	9E	DD 9E d	FD 9E d	DE n
AND	A7	A0	A1	A2	A3	A4	A5	A6	DD A6 d	FD A6 d	E6 n
XOR	AF	A8	A9	AA	AB	AC	AD	AE	DD AE d	FD AE d	EE n
OR	B7	B0	B1	B2	B3	B4	B5	B6	DD B6 d	FD B6 d	F6 n
CP	BF	B8	B9	BA	BB	BC	BD	BE	DD BE d	FD BE d	FE n
INC	3C	04	0C	14	1C	24	2C	34	DD 34 d	FD 34 d	
DEC	3D	05	0D	15	1D	25	2D	35	DD 35 d	FD 35 d	

Table 6. 8-Bit Arithmetic & Logic.

	SOURCE & DESTINATION									
MNEMONIC	A	B	C	D	E	H	L	(HL)	(IX + d)	(IY + d)
RLC	07	00	01	02	03	04	05	06	d 06	d 06
RRC	0F	08	09	0A	0B	0C	0D	0E	d 0E	d 0E
RL	17	10	11	12	13	14	15	16	d 16	d 16
RR	1F	18	19	1A	1B	1C	1D	1E	d 1E	d 1E
SLA	27	20	21	22	23	24	25	26	d 26	d 26
SRA	2F	28	29	2A	2B	2C	2D	2E	d 2E	d 2E
SRL	3F	38	39	3A	3B	3C	3D	3E	d 3E	d 3E
RLD								ED 6F		
RRD								ED 67		
RLCA	07									
RRCA	0F									
RLA	17									
RRA	1F									

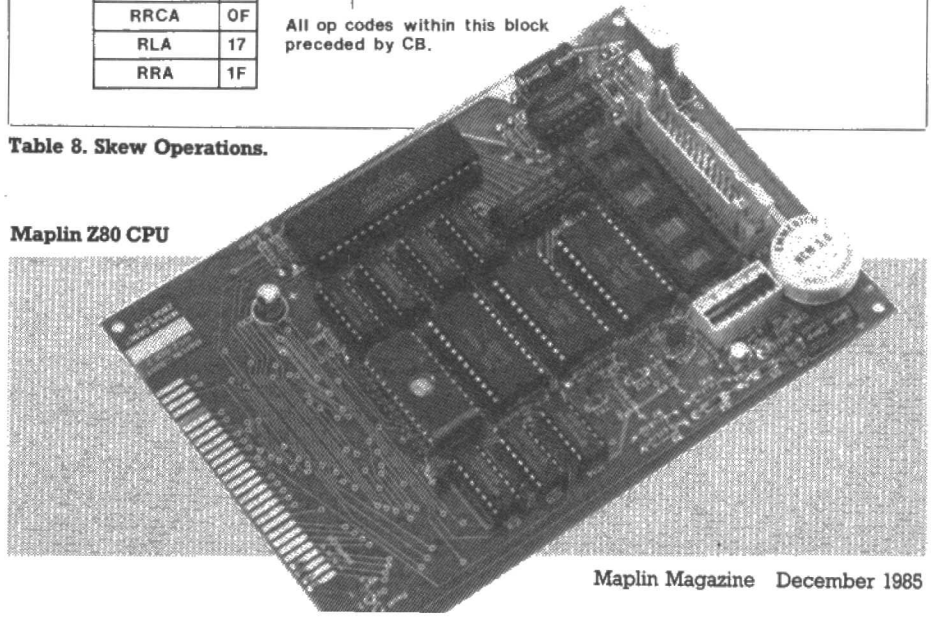
Prefix these op codes by FD CB.

Prefix these op codes by DD CB.

All op codes within this block preceded by CB.

Table 8. Skew Operations.

Maplin Z80 CPU



MNEMONIC		REGISTER ADDRESSING							REG. IND.	INDEXED	
	BIT	A	B	C	D	E	H	L	(HL)	(IX + d)	(IY + d)
BIT	0	47	40	41	42	43	44	45	46	46	46
	1	4F	48	49	4A	4B	4C	4D	4E	4E	4E
	2	57	50	51	52	53	54	55	56	56	56
	3	5F	58	59	5A	5B	5C	5D	5E	5E	5E
	4	67	60	61	62	63	64	65	66	66	66
	5	6F	68	69	6A	6B	6C	6D	6E	6E	6E
	6	77	70	71	72	73	74	75	76	76	76
	7	7F	78	79	7A	7B	7C	7D	7E	7E	7E
RES	0	87	80	81	82	83	84	85	86	86	86
	1	8F	88	89	8A	8B	8C	8D	8E	8E	8E
	2	97	90	91	92	93	94	95	96	96	96
	3	9F	98	99	9A	9B	9C	9D	9E	9E	9E
	4	A7	A0	A1	A2	A3	A4	A5	A6	A6	A6
	5	AF	A8	A9	AA	AB	AC	AD	AE	AE	AE
	6	B7	B0	B1	B2	B3	B4	B5	B6	B6	B6
	7	BF	B8	B9	BA	BB	BC	BD	BE	BE	BE
SET	0	C7	C0	C1	C2	C3	C4	C5	C6	C6	C6
	1	CF	C8	C9	CA	CB	CC	CD	CE	CE	CE
	2	D7	D0	D1	D2	D3	D4	D5	D6	D6	D6
	3	DF	D8	D9	DA	DB	DC	DD	DE	DE	DE
	4	E7	E0	E1	E2	E3	E4	E5	E6	E6	E6
	5	EF	E8	E9	EA	EB	EC	ED	EE	EE	EE
	6	F7	F0	F1	F2	F3	F4	F5	F6	F6	F6
	7	FF	F8	F9	FA	FB	FC	FD	FE	FE	FE

Prefix all op codes in this block by CB.

Prefix all op codes in this column by DD CB d.

Prefix all op codes in this column by FD CB d.

Table 9. Bit Manipulation Group.

MNEMONIC	ADD. MODE	OPERAND	CONDITION: UN CON.	CARRY	NON CARRY	ZERO	NON ZERO	PARITY even	PARITY odd	SIGN neg.	SIGN pos.	REG. B ≠ 0
JP	IMM. EXT.	nn	C3 nn	DA nn	D2 nn	CA nn	C2 nn	EA nn	E2 nn	FA nn	F2 nn	
JR	RELATIVE	PC + e	18 e−2	38 e−2	30 e−2	28 e−2	20 e−2					
JP	REG. IND.	(HL)	E9									
		(IX)	DD E9									
		(IY)	FD E9									
CALL	IMM. EXT.	nn	CD nn	DC nn	D4 nn	CC nn	C4 nn	EC nn	E4 nn	FC nn	F4 nn	
DJNZ	RELATIVE	PC + e										10 e−2
RET	REG. IND.	(SP) (SP + 1)	C9	D8	D0	C8	C0	E9	E0	F8	F0	
RETI	REG. IND.	(SP) (SP + 1)	ED 4D									
RETN	REG. IND.	(SP) (SP + 1)	ED 45									

Table 11. Jump Instructions.

MNEMONIC	OP CODE
DAA	27
CPL	2F
NEG	ED 44
CCF	3F
SCF	37

Table 10. General Purpose AF Operations.

			SOURCE: PORT ADDRESS IMM. (n)	SOURCE: PORT ADDRESS REG. IND. (c)
INPUT DESTINATION	IN	A	DB	78
		B		40
		C		48
		D		50
		E		58
		H		60
		L		68
	INI	REG. IND. (HL)		A2
	INIR			B2
	IND			AA
	INDR			BA

Block commands

Prefix all op codes in this column with ED.

Table 14. Input Group.

MNEMONIC	OP CODE
NOP	00
HALT	76
DI	F3
EI	FB
IM0	ED 46
IM1	ED 56
IM2	ED 5E

Table 15. Miscellaneous CPU Group.

	RST0	RST8	RST16	RST24	RST32	RST40	RST48	RST56
CALL ADDRESS	&0000	&0008	&0010	&0018	&0020	&0028	&0030	&0038
OP CODE	C7	CF	D7	DF	E7	EF	F7	FF

Table 12. Restart Group.

		SOURCE: PORT ADDRESS	REGISTER A	B	C	D	E	H	L	REG. IND. (HL)
OUT	IMM.	(n)	D3 n							
	REG. IND.	(c)	79	41	49	51	59	61	69	
OUTI	REG. IND.	(c)								A3
OTIR		(c)								B3
OUTD		(c)								A8
OTDR		(c)								B8

Block commands

N.B. Prefix ALL op codes in this table with ED.

Table 13. Output Group.

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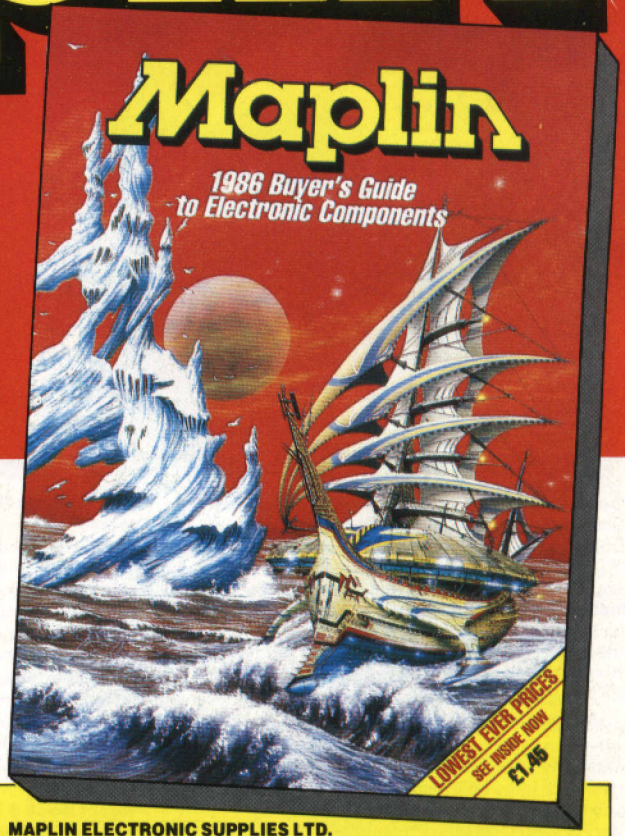

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